

**A HIGH PERFORMANCE OPERATIONAL AMPLIFIER
UTILIZING FIELD EFFECT INPUT DEVICES
COMPATIBLE WITH
INTEGRATED CIRCUIT FABRICATION TECHNIQUES**

By

James Elbert Thompson

**A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science in Engineering**

ARIZONA STATE UNIVERSITY

June, 1968

A HIGH PERFORMANCE OPERATIONAL AMPLIFIER
UTILIZING FIELD EFFECT INPUT DEVICES
COMPATIBLE WITH
INTEGRATED CIRCUIT FABRICATION TECHNIQUES

By

James Elbert Thompson

has been approved

May, 1967

APPROVED:

SC Gupta Chairman
J. Barkson
W. Zimmerman
William Lewis

Supervisory Committee

ACCEPTED:

Thomas E. Tice
Department Chairman

W. J. Bank
Dean, Graduate College

ACKNOWLEDGEMENT

The author wishes to express his gratitude to Professor S. C. Gupta for supervising the preparation of this paper. Thanks are also due to Motorola, Inc., Semiconductor Products Division, for the use of its laboratory facilities; to J. S. Foster for construction of the experimental model and assistance with measurements; to E. L. Long for assistance in obtaining experimental field-effect devices; and to Mrs. Anne Dana for typing the final manuscript.

TABLE OF CONTENTS

CHAPTER	PAGE
I. INTRODUCTION.....	1
Conventional Operational Amplifiers.....	1
Basic Integrable Configuration.....	3
Development of Desired Performance.....	3
II. D.C. CIRCUIT DESIGN.....	6
Common Mode Analysis.....	6
Computation of D.C. Differential Voltage Gain....	11
III. HIGH FREQUENCY EFFECTS.....	17
Derivation of High Frequency Model.....	17
Need for Compensation.....	20
Techniques of Compensation.....	21
Compensation by Pole Splitting.....	21
Improvements due to Pole Splitting.....	23
IV. ADDITION OF SPECIAL PURPOSE FEATURES.....	24
Class B Output Stage.....	24
Short Circuit Protection.....	27
V. EXPERIMENTAL RESULTS.....	30
Experimental Model.....	30
Definition of Operational Amplifier Parameters...	30
D.C. Characteristics.....	34

TABLE OF CONTENTS (Cont'd)

CHAPTER	PAGE
High Frequency Characteristics.....	34
Class B Stage and Short Circuit Protection.....	37
Discussion of Experimental Results.....	37
VI. MONOLITHIC REALIZATION.....	38
Devices.....	38
Resistors.....	38
Monolithic Improvements.....	40
VII. SUMMARY.....	41
BIBLIOGRAPHY.....	43

LIST OF TABLES

TABLE	PAGE
I. DEFINITION OF OPERATIONAL AMPLIFIER PARAMETERS.....	32
II. EXPERIMENTAL D.C. CHARACTERISTICS.....	35

LIST OF FIGURES

FIGURE	PAGE
1. Two conventional level shifting techniques.....	2
2. Basic configuration for operational amplifier utilizing P-channel FET input devices.....	4
3. Lateral PNP current source essentially independent of β_p	7
4. Common mode loop.....	7
5. Integrated circuit diode.....	9
6. Current source I_1	9
7. Operational amplifier with component values assigned and quiescent operating conditions indicated.....	12
8. D.C. models.....	13
9. Model for calculation of overall D.C. differential gain.....	15
10. Model for amplifier at high frequencies.....	18
11. Conventional complementary class B stage.....	25
12. Lateral PNP/NPN class B stage.....	25
13. Distortion of Figure 12 circuit.....	25
14. Transistor matching to reduce distortion.....	26
15. Resistive drop reduces current consumption.....	26
16. Short circuit protection devices.....	28
17. Final circuit diagram of experimental model.....	31
18. Operational amplifier block diagram.....	33

FIGURE	PAGE
19. D.C. Gain versus temperature.....	33
20. Gain versus frequency.....	36
21. Monolithic processing steps.....	39

CHAPTER I

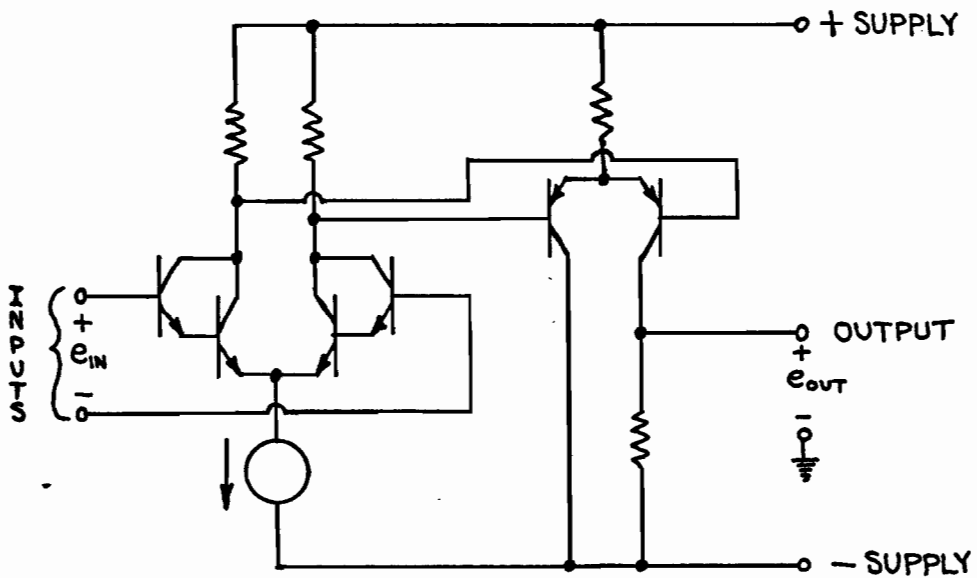
INTRODUCTION

Integrated circuit processing capabilities have restricted the circuit designer to an all NPN bipolar transistor technology, with the result that contemporary integrated operational amplifiers have suffered from two serious deficiencies: 1) large input bias currents with associated high drift; and 2) low gain-bandwidth products, with closed loop stability obtainable only at the expense of large externally connected compensation capacitors. In this paper an operational amplifier utilizing field effect input devices is developed which has very low input bias currents, high gain, moderately large gain-bandwidth product, very small compensation capacitors, and compatibility with integrated circuit fabrication techniques.

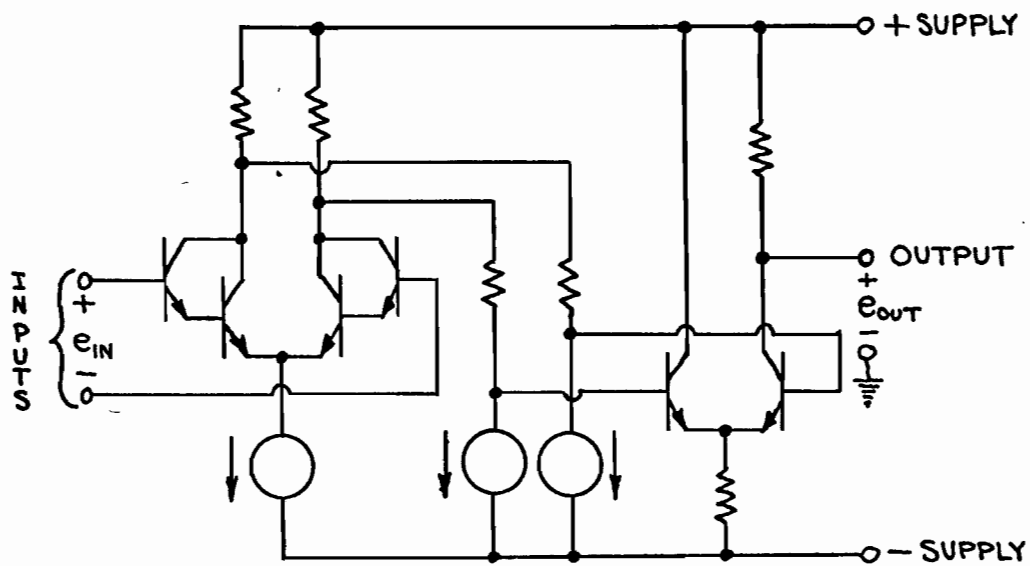
Conventional Operational Amplifiers

Figure 1 shows two conventional basic operational amplifier circuits. Both configurations shown have the high input bias currents inherent to bipolar technology.

Figure 1(a) uses an NPN-PNP cascade to accomplish the operational requirement that when $e_{IN} = 0$, then $e_{OUT} = 0$. This basic circuit form would result in a good operational amplifier if it were not for the fact that good PNP transistors are not available with present integrated circuit processing techniques. This circuit can be fabricated using a lateral PNP-NPN composite [1], but present lateral PNP's have



(a)



(b)

Figure 1. Two conventional level shifting techniques

such low f_t 's that gain-bandwidth product suffers.

Figure 1(b) shows a "level shifting" technique [2] using a resistor and a constant current source. This circuit avoids the use of PNP devices altogether. In a typical situation the resistor must be relatively large and the stray capacitances associated with the current source are significant. Again, frequency response suffers.

Basic Integrable Configuration

Figure 2 shows the basic configuration for the circuit to be discussed in this paper. The use of P-channel junction field effect devices cascaded with an NPN differential amplifier easily allows satisfying the desired input-output restraint that $e_{OUT} = 0$ when $e_{IN} = 0$. The use of current source loading on the FET's and the darlington input connection for the NPN differential amplifier yields high gain with only two stages. It will be shown that it is a simple matter to apply compensation to this circuit such that single dominant pole response can be obtained. With field effect input devices this circuit will have input bias currents which are several orders of magnitude smaller than that attainable with bipolar devices.

Development of Desired Performance

Derivation of the circuit restraints required to yield the desired input-output characteristics of the amplifier will be performed in four steps: 1) A common mode analysis will be accomplished first, since the requirement for stable device D. C. operating points places the most stringent restrictions on circuit values. 2) D. C. differential voltage gain will then be computed. 3) A high frequency

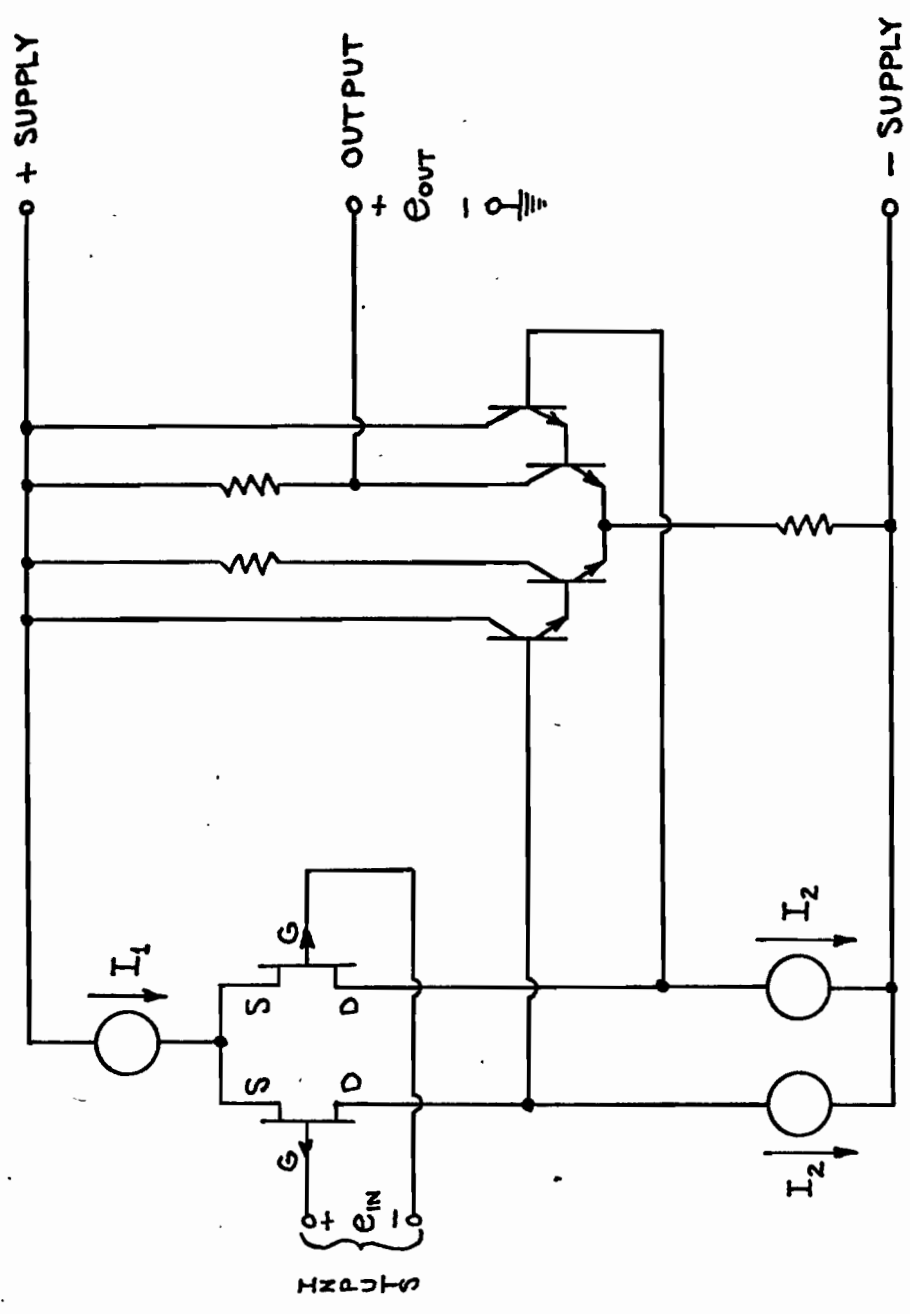


Figure 2. Basic configuration for operational amplifier utilizing P-channel FET input devices

model for the amplifier will be shown, and a method for compensating the amplifier will be developed. 4) Finally it will be shown how special purpose features may be easily added to the basic amplifier.

Theoretical performance is compared with experimental results obtained from a model constructed using integrated circuit devices. Techniques required for complete realization of the amplifier in monolithic form is then discussed.

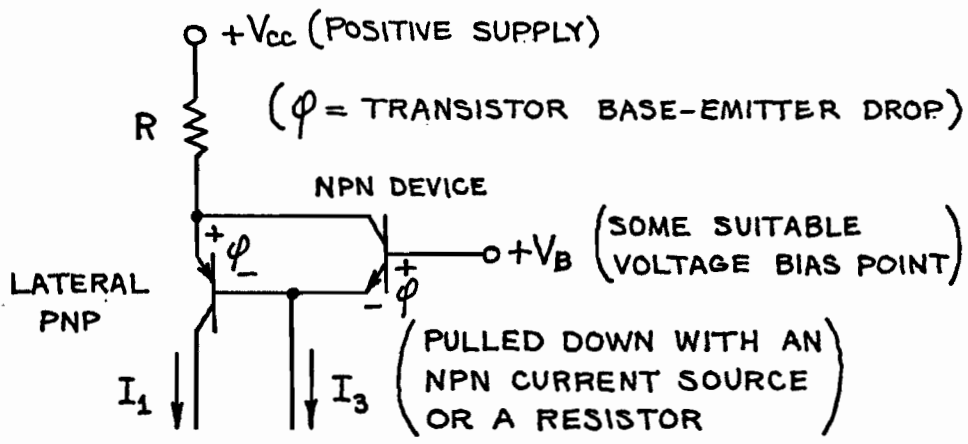
CHAPTER II

D.C. CIRCUIT DESIGNCommon Mode Analysis

Referring to Figure 2 it can be seen that there are three current sources essential to the proper functioning of this amplifier. Current source I_1 is necessary to give proper rejection to any signal common to both inputs (common mode rejection). Current sources, I_2 , are required to provide a high load impedance for the field effect drain circuits to realize high voltage gain from the stage.

Current sources, I_2 , are easily realized using ordinary NPN transistors. Current source I_1 presents a problem since this current polarity flowing from the positive supply requires a PNP device. As was mentioned previously, high quality PNP's are not available with present integrated circuit fabrication techniques. However, it is possible, in this instance, to use a lateral PNP device for this current source even though lateral PNP betas may be close to unity [1]. Figure 3 shows one possible method which is independent of lateral beta, β_p , if $\beta_p \geq \frac{I_1}{I_3}$. (Buried layer technology is assumed so that substrate currents may be ignored).

For the NPN differential amplifier to have the proper quiescent operating conditions, the current sources must be matched such that $I_1 = 2I_2$. This is best accomplished using some form of feedback loop. Consider, for example, the configuration shown in Figure 4. (Differ-



$$I_1 = \frac{V_{cc} - V_B}{R} - I_3, \text{ FOR } \beta_P \geq \frac{I_1}{I_3}.$$

Figure 3. Lateral PNP current source essentially independent of β_p

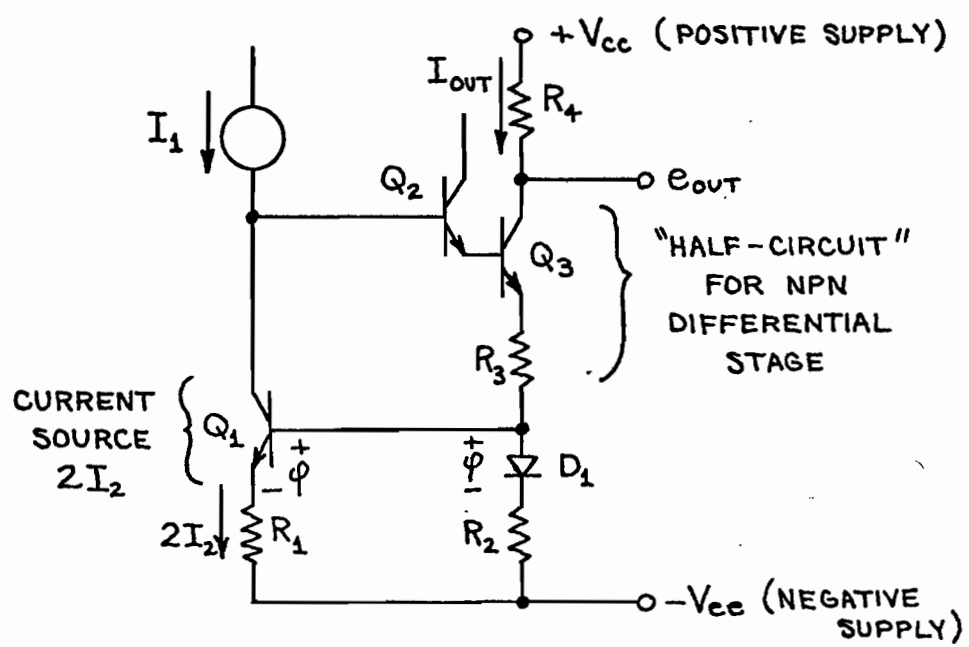


Figure 4. Common mode loop

ential e_{IN} is assumed zero, thus balanced circuits have been bisected [3] or ignored [4] where applicable, yielding a "half-circuit" which greatly simplifies analysis.)

Referring to the figure it can be seen that if $I_1 > 2I_2$, the voltage at the base of device Q_2 must rise, causing more current to flow through the network composed of R_3 , D_1 , and R_2 . Since the current flow in this network determines the current $2I_2$, $2I_2$ will increase until it equals I_1 (less the base current demand of device Q_2).

In addition to establishing the current source $2I_2$ at its proper value, this loop also sets the value of the quiescent current, I_{OUT} , for the stage composed of Q_2 and Q_3 . Since the circuit is to be fabricated with integrated circuit techniques, it can be assumed that base-emitter voltage drops match quite closely. Therefore, the drop across diode D_1 (see Figure 5) matches the base-emitter drop of device Q_1 , and the quiescent current, I_{OUT} , is restrained to be

$$I_{OUT} = 2 \frac{R_1}{R_2} I_2. \quad (1)$$

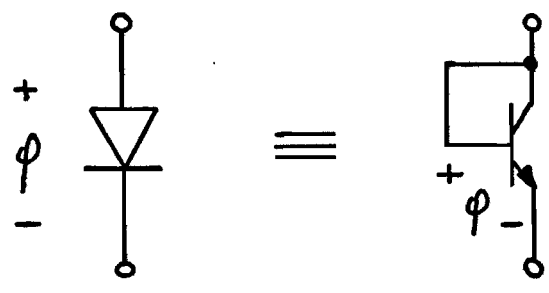
But since the circuit forces $I_1 = 2I_2$, then

$$I_{OUT} = \frac{R_1}{R_2} I_1. \quad (2)$$

Referring to Figure 4 again, it can be seen that

$$e_{OUT} = V_{CC} - I_{OUT} R_4. \quad (3)$$

Substituting the value of I_{OUT} obtained in Equation (2) into Equation (3) we find that



$\phi = \text{BASE-EMITTER DROP}$

Figure 5. Integrated circuit diode

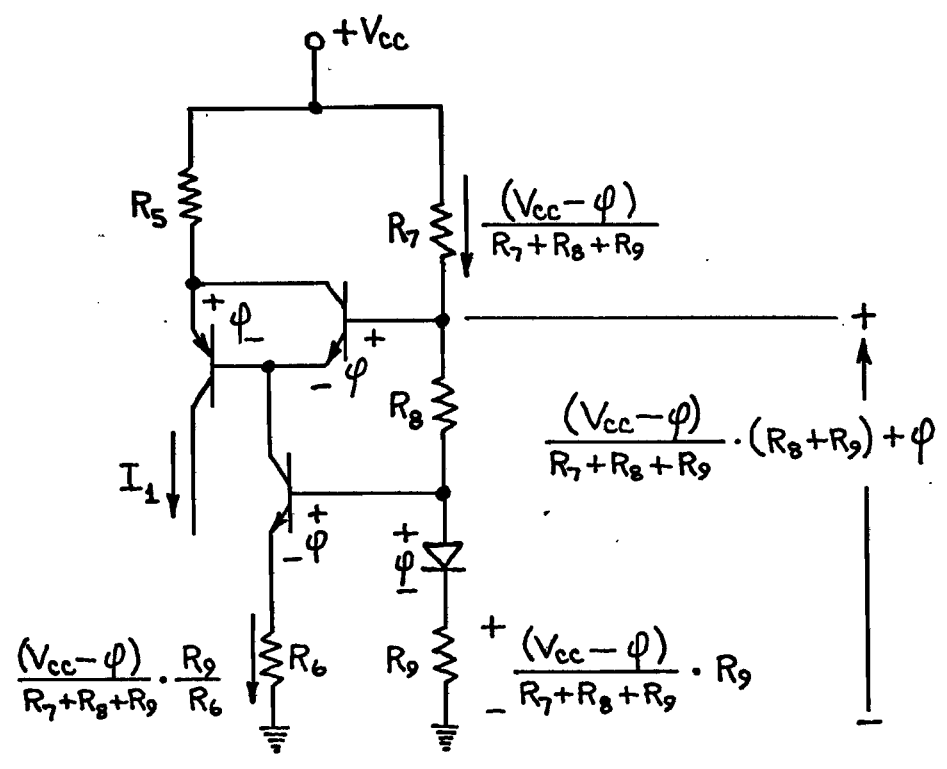


Figure 6. Current source I_1

$$e_{\text{OUT}} = V_{\text{CC}} - \frac{R_1}{R_2} R_4 I_1. \quad (4)$$

In the foregoing discussion we have found that if current I_1 is determined, quiescent currents $2I_2$ and I_{OUT} and output voltage e_{OUT} are all established at values directly related to I_1 . It follows then that if e_{OUT} is desired to be some specific function of power supply voltages and circuit parameters, I_1 must contain this specific function.

In this typical situation, with differential voltage $e_{\text{IN}} = 0$, it is desired that the output voltage be independent of supply voltages and be offset in the positive direction one base-emitter voltage drop ($+\phi$), so as to accommodate the addition of a Class B output stage. (The net result would be $e_{\text{OUT}} = 0$, independent of supplies and temperature.)

Now consider the circuit configuration shown in Figure 6 for the current source, I_1 . It is easily derived that

$$I_1 = \frac{(V_{\text{CC}} - \phi)}{R_7 + R_8 + R_9} \cdot \left(\frac{R_7}{R_5} - \frac{R_9}{R_6} \right). \quad (5)$$

But

$$e_{\text{OUT}} = V_{\text{CC}} - \frac{R_1}{R_2} R_4 I_1 \quad (4)$$

thus

$$e_{\text{OUT}} = V_{\text{CC}} - \frac{(V_{\text{CC}} - \phi)}{R_7 + R_8 + R_9} \cdot \left(\frac{R_7}{R_5} - \frac{R_9}{R_6} \right) \cdot \frac{R_1}{R_2} \cdot R_4 \quad (6)$$

or

$$e_{\text{OUT}} = V_{\text{CC}} \left[1 - \left(\frac{R_7}{R_5} - \frac{R_9}{R_6} \right) \cdot \left(\frac{R_1}{R_2} \right) \cdot \left(\frac{R_4}{R_7 + R_8 + R_9} \right) \right] \\ + \phi \left[\left(\frac{R_7}{R_5} - \frac{R_9}{R_6} \right) \cdot \left(\frac{R_1}{R_2} \right) \cdot \left(\frac{R_4}{R_7 + R_8 + R_9} \right) \right] \quad (7)$$

Note that if

$$\left(\frac{R_7}{R_5} - \frac{R_9}{R_6}\right) \cdot \left(\frac{R_1}{R_2}\right) \cdot \left(\frac{R_4}{R_7 + R_8 + R_9}\right) = 1 \quad (8)$$

then

$$e_{\text{OUT}} = +\phi \quad (9)$$

independent of positive supply V_{cc} (and negative supply V_{ee} since it does not even enter the equations).

There is infinite variability in our choice of values to satisfy (8), but the values must be chosen with some regard to power consumption and internal circuit nodal voltages. The following set of restraints has been found valid for all practical operating conditions.

$$\begin{aligned} \frac{R_7}{R_5} &= 3 & \frac{R_1}{R_2} &= 2 \\ \frac{R_4}{R_7 + R_8 + R_9} &= \frac{1}{2} & \frac{R_9}{R_6} &= 2 \end{aligned} \quad (10)$$

Figure 7 shows the circuit developed from these restraints. The circuit design is essentially complete, except for the addition of special purpose features. The differential characteristics of this circuit must now be analyzed to determine adequacy of gain and frequency response.

Computation of D.C. Differential Voltage Gain

D.C. differential voltage gain can be computed by utilizing a model for the FET-NPN differential cascade. At D.C. the simple models shown in Figure 8 are applicable. Only half of each differential stage need be considered for the calculations since the bisection

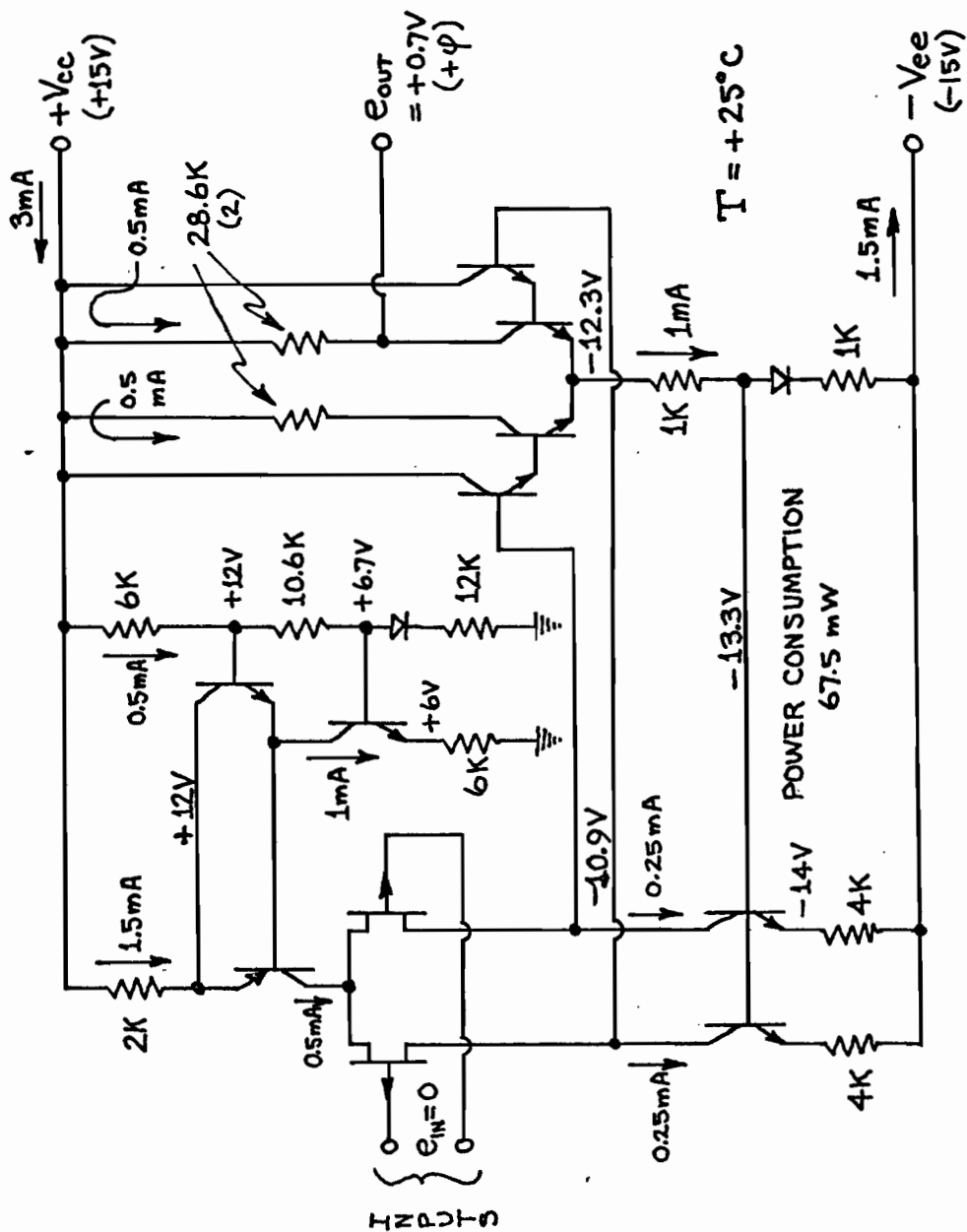
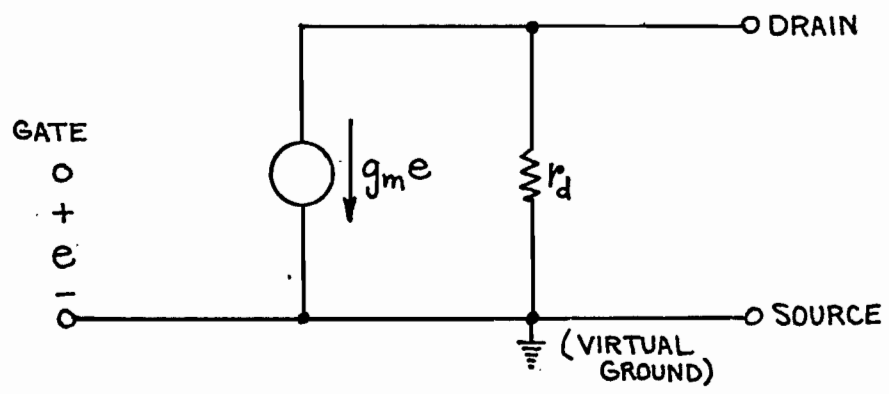
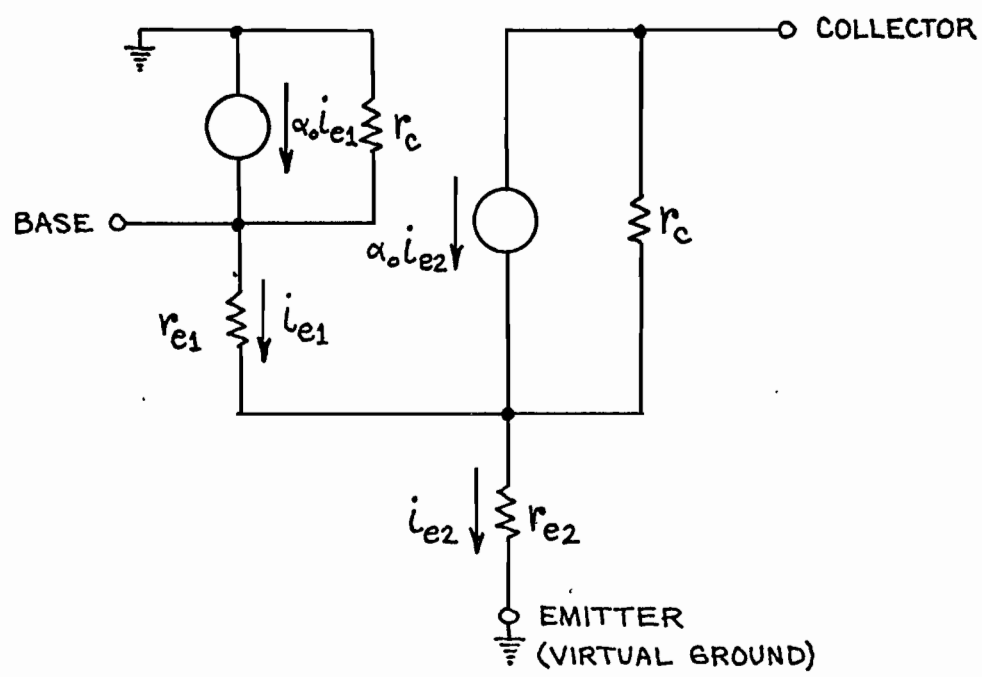


Figure 7. Operational amplifier with component values assigned and quiescent operating conditions indicated



(a) Field-effect device



(b) NPN Darlington

Figure 8. D.C. models

theorem [3] can be applied. Combining these individual stage models and adding appropriate load impedances we obtain the overall model shown in Figure 9. Model parameters are defined as follows:

- g_m - transconductance of field effect device
- r_d - output resistance of field effect drain
- r_c - output resistance of NPN collectors
- $r_{e1,2}$ - emitter resistances of NPN devices
- α_o - current gain of NPN devices
- R_L - load impedance

(Note that r_c inserted between the two device models is due to the collector impedance of the current source load in the field effect drain circuit.)

Developing an input-output equation from this model we arrive at

$$\frac{e_{OUT}}{e_{IN}} = \frac{\beta_o^2 g_m R_L r_p}{r_p + 2\beta_o^2 r_{e2}} \quad (11)$$

Several approximations and substitutions have been used to derive this result:

$$\begin{aligned} r_p &= r_d \parallel \frac{r_c}{2} \\ \alpha_o r_c &\gg r_{e2} \\ r_c &\gg R_L \\ (1 - \alpha_o) r_p &\gg r_{e1} \\ \beta_o &= \frac{\alpha_o}{1 - \alpha_o} \end{aligned} \quad (12)$$

Before proceeding further it must be noted that by utilizing the bi-

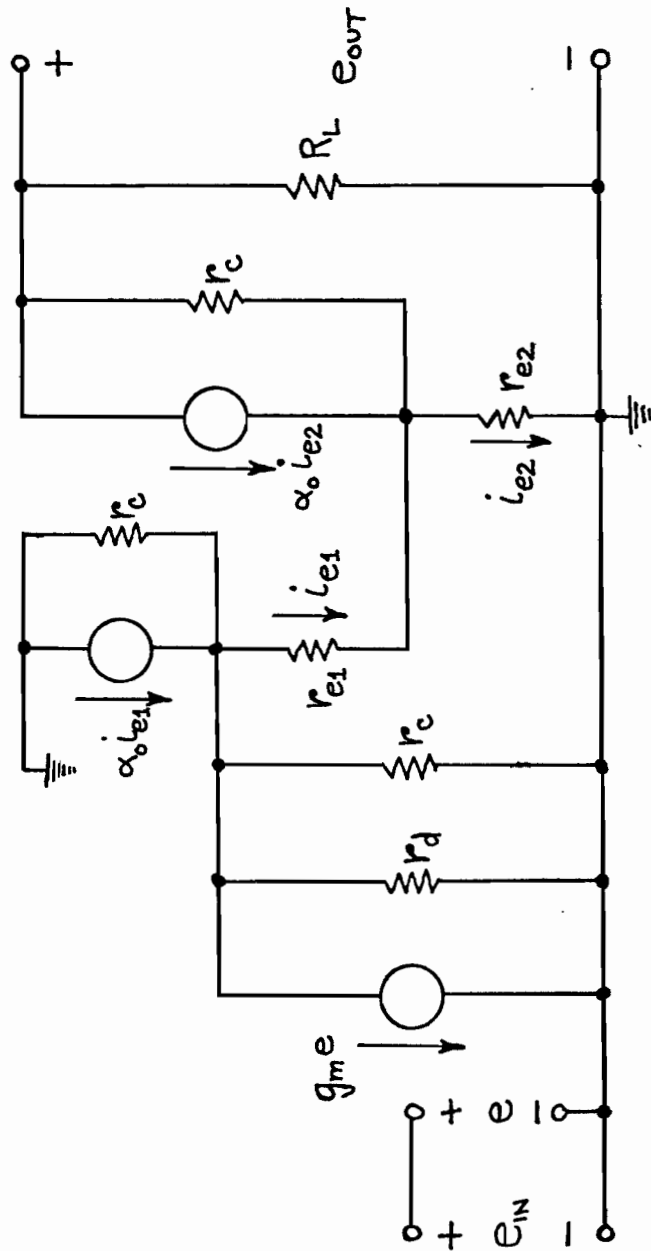


Figure 9. Model for calculation of overall D.C. differential gain

section theorem we have assumed differential output, as well as input voltages. In this case the output signal is taken from only one side of the second differential amplifier, and the result of equation (11) must be divided by two. Therefore, the overall voltage gain of the amplifier is given by

$$\frac{e_{OUT}}{e_{IN}} = \frac{1}{2} \cdot \frac{\beta_o^2 g_m R_L r_p}{r_p + 2\beta_o^2 r_{e2}} \quad (13)$$

Approximate element values for the devices used are:

$$g_m = 600 \mu\text{mhos}$$

$$r_d \approx 4 \text{ MEG}$$

$$r_c \approx 5 \text{ MEG}$$

$$r_p = r_d \parallel \frac{r_c}{2} \approx 2 \text{ MEG}$$

$$R_L = 28 \text{ K}$$

$$\beta_o = 50$$

$$r_{e2} = 52$$

Applying these values to Equation (13) we obtain

$$\frac{e_{OUT}}{e_{IN}} = 21,000$$

or approximately 86 db of gain.

CHAPTER III

HIGH FREQUENCY EFFECTSDerivation of High Frequency Model

The most useful properties of operational amplifiers are developed by applying a feedback loop from the output to the inverting input (negative feedback). Therefore, the high frequency characteristics of the amplifier must be examined to ensure closed loop stability under all possible feedback conditions. For general feedback networks and unconditional stability the amplifier open loop gain must decrease to the desired closed loop gain at a rate no greater than 6db octave. This restricts the amplifier to single dominant pole response in the gain range of interest.

Figure 10 shows a composite model for the amplifier which is adequate for analyzing high frequency behavior below approximately 10MC. This model was derived by combining a model for the field-effect input device [5] with a "hybrid-pi" model [6] for the darlington-connected second stage [7]. Emitter transition capacitance and frequency effects inherent in transistor β have been ignored, since their effects are not significant below 10MC. Low source impedance has been assumed to eliminate the source pole from the analysis and to allow lumping field-effect device capacitances together. Parameter definitions are as follows:

g_m - field-effect device transconductance

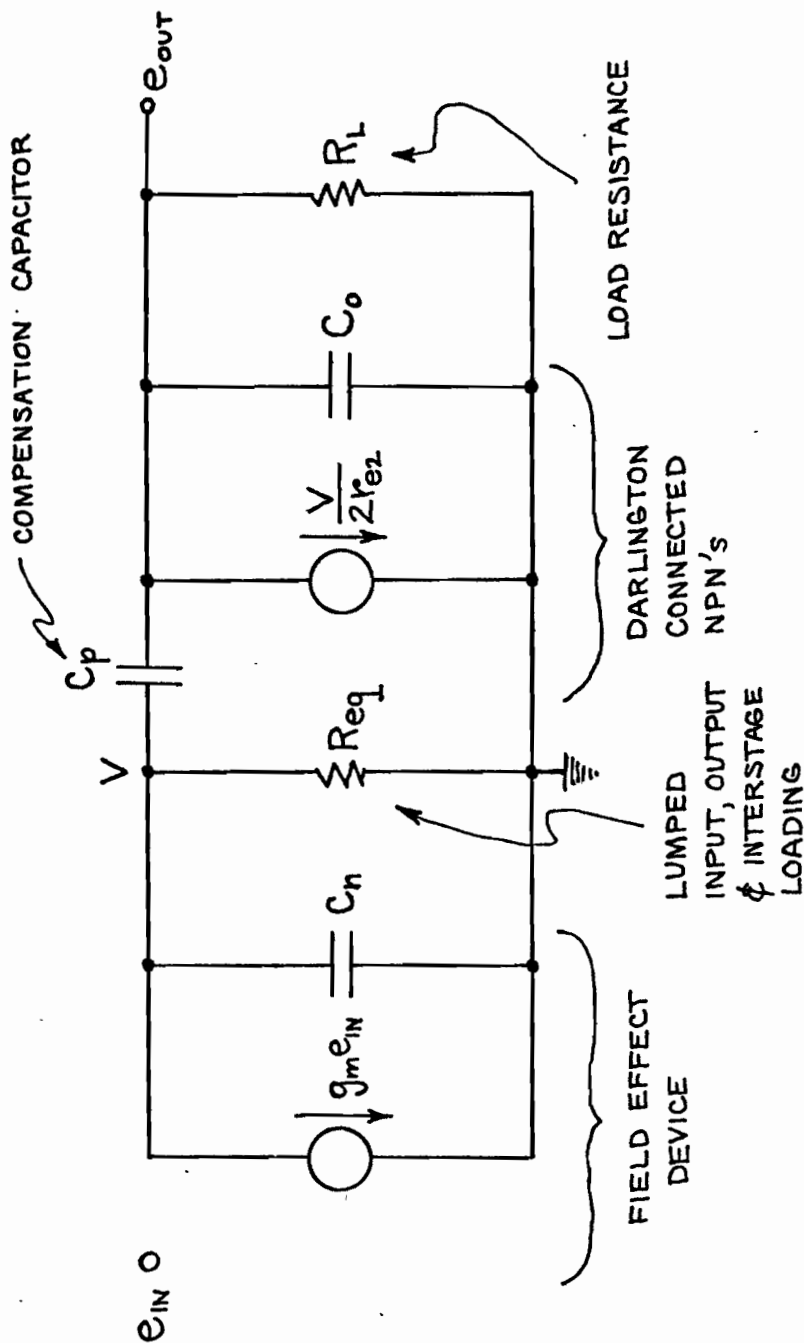


Figure 10. Model for amplifier at high frequencies

$$C_n = C_{dg} + C_{ds} + 2C_c$$

C_{dg} - drain to gate capacitance of field-effect device

C_{ds} - drain to source capacitance of field-effect device

C_c - collector to base capacitance of NPN device

$$R_{eq} = r_d \parallel \left[\frac{r_c}{2} \parallel 2\beta_o^2 r_{e2} \right]$$

r_d - drain resistance of field-effect device

r_c - collector resistance of NPN device

r_{e2} - emitter resistance of second NPN device

β_o - common emitter D.C. current gain of NPN device

$$C_o = C_s + C_c$$

C_s - collector to substrate capacitance of NPN device

R_L - load resistance

C_p - compensation capacitor

By analyzing this model the open loop pole locations can be found from the roots of the characteristic equation

$$s^2 R_L R_{eq} (C_o + C_p)(C_n + C_p) + s \left[R_L (C_o + C_p) + R_{eq} (C_n + C_p) + \frac{R_L R_{eq}}{2r_{e2}} C_p \right] + 1 = 0. \quad (14)$$

When $C_p = 0$ this equation reduces to

$$s^2 R_L R_{eq} C_o C_n + s \left[R_L C_o + R_{eq} C_n \right] + 1 = 0 \quad (15)$$

which can be solved for the uncompensated pole locations. Assuming widely separated poles [8], the poles are given by

$$p_1 = \frac{1}{R_L C_o + R_{eq} C_n} \quad (16)$$

$$P_2 = \frac{R_L C_o + R_{eq} C_n}{R_L R_{eq} C_o C_n} \quad (17)$$

Applying the values

$$R_L = 28 \text{ K}$$

$$C_o = 2.5 \text{ pf}$$

$$R_{eq} = 250 \text{ K}$$

$$C_n = 10 \text{ pf}$$

we obtain

$$P_1 = 63.6 \text{ KC}$$

and

$$P_2 = 2.22 \text{ MC}$$

as the open loop pole locations with no compensation.

The minimum attainable unconditionally stable closed loop gain, G_{CLMIN} , is approximately related to the amplifier open loop gain, G_{OL} , and the pole locations, p_1 and p_2 :

$$G_{CLMIN} \text{ (db)} = G_{OL} \text{ (db)} - \frac{P_2}{P_1} \text{ (db)}. \quad (18)$$

For this amplifier in uncompensated form with

$$G_{OL} = 86 \text{ db}$$

$$\frac{P_2}{P_1} = 34.9 \text{ (30.8 db)}$$

then $G_{CLMIN} = 86 - 30.8 = 55.2 \text{ db}$.

Need for Compensation

In typical usage of operational amplifiers it is often required that $G_{CLMIN} = 0 \text{ db}$. To accomplish this degree of stable feedback requires the application of frequency compensation to adequately separ-

ate the poles p_1 and p_2 .

Techniques of Compensation

The conventional approach to this problem would be to pad capacitance at the node determining pole p_1 to further narrow-band it. Since p_2 and p_1 must be separated by 86 db, p_1 must be reduced to approximately 100 cps for unconditional stability at $G_{CLMIN} = 0$ db. A capacitor value of approximately .006 μ f would be required from each field effect drain to ground to accomplish this compensation. Such a large value capacitor will have extremely detrimental effects on amplifier slew rate (see later discussion). In addition, the gain-bandwidth product of the amplifier has not been improved by the compensation but is still limited by the location of pole p_2 to 2.22 MC.

Compensation by Pole Splitting

Now let us consider the compensating effects of capacitor C_p . Returning to Equation (14) and assuming widely separated poles [8], the pole locations are now given by

$$p_1 = \frac{1}{R_L(C_o + C_p) + R_{eq}(C_n + C_p) + \frac{R_L R_{eq}}{2r_{e2}} C_p} \quad (19)$$

and

$$p_2 = \frac{R_L(C_o + C_p) + R_{eq}(C_n + C_p) + \frac{R_L R_{eq}}{2r_{e2}} C_p}{R_L R_{eq} (C_o + C_p)(C_n + C_p)} \quad (20)$$

For

$$\frac{2r_{e2}}{R_L} C_n < C_p < C_n \quad (21)$$

Equations (19) and (20) can be simplified to

$$P_1 = \frac{2r_{e2}}{R_L R_{eq} C_p} \quad (22)$$

$$P_2 = \frac{C_p}{2r_{e2} C_o C_n} \quad (23)$$

A very interesting result of these equations is that as C_p increases, p_1 is narrow-banded and p_2 is broad-banded. This "pole-splitting" technique [9] can therefore result in improved gain-bandwidth product, particularly when it is desired to have $G_{CLMIN} = 0$ db.

It must be pointed out here that gain-bandwidth-product improvement obtained in this fashion is limited due to a cluster of essentially immobile poles located just above 10 MC. These poles are due to transistor transition capacitance and dependence of transistor β on frequency, and were ignored during development of the high frequency model. Since pole p_2 is pushed out well beyond 10 MC by C_p , let us assume the existence of a new band-limiting pole $p_3 = 10$ MC. The minimum attainable stable closed loop gain will be given by

$$G_{CLMIN} \text{ (db)} = G_{OL} \text{ (db)} - \frac{P_3}{P_1} \text{ (db)} \quad (24)$$

or

$$G_{CLMIN} = G_{OL} \frac{P_1}{P_2} \text{ (ratio gain)} \quad (25)$$

Equation (25) may then be used to find the required location of pole p_1 for the desired closed loop gain G_{CLMIN} .

Consider for example $G_{CLMIN} = 1$.

Since

$$p_1 = \frac{G_{CLMIN}}{G_{OL}} p_3 \quad (26)$$

then

$$p_1 = \frac{1}{2 \times 10^4} \times 10^7$$

or

$$p_1 = 500 \text{ cps}$$

The compensation capacitor, C_p , can be found by rewriting Equation (22) such that

$$C_p = \frac{2r_{e2}}{R_L R_{eq} p_1} \quad (27)$$

For the situation under discussion $C_p = 4.5 \text{ pf}$.

Improvements due to Pole Splitting

Three significant improvements over conventional compensation techniques have been realized with this "pole-splitting" technique:

- 1) gain-bandwidth-product has been improved by a factor of 5 for the $G_{CLMIN} = 1$ case (the worst situation),
- 2) the compensation capacitor value is much reduced, and as a result,
- 3) slew rate capability will be much improved (see later discussion).

CHAPTER IV

ADDITION OF SPECIAL PURPOSE FEATURESClass B Output Stage

It is often desirable to have in an operational amplifier the capability of driving a 1 K load through a ± 10 volt swing. If high quiescent power consumption is to be avoided a class B output stage is required.

Figure 11 shows a conventional complementary class B output stage. An effective PNP device replacement can be accomplished with a lateral PNP/NPN composite as shown in Figure 12. However, this stage has one serious flaw - distortion. The input signal must move through two base-emitter drops to switch conduction from NPN device to PNP device and vice versa. This causes distortion of the form shown in Figure 13.

This distortion can be reduced significantly by employing two transistors connected as diodes as in Figure 14. Because transistor base-emitter drops can be made to match in integrated circuit fabrication this stage has both the NPN and PNP device in their active regions simultaneously to create essentially a class AB operation. With transistor matching the output stage will then consume the same quiescent current as flows in the output collector of the second differential stage of the operational amplifier. Since this quiescent consumption can be as much as 30 mW during negative output swing

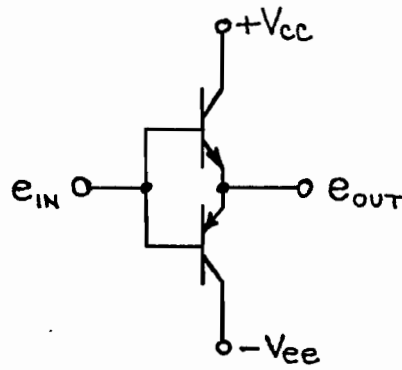


Figure 11. Conventional complementary class B stage

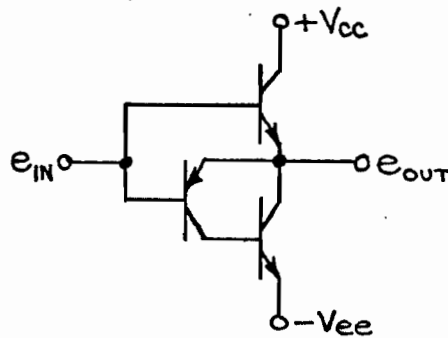


Figure 12. Lateral PNP/NPN class B stage

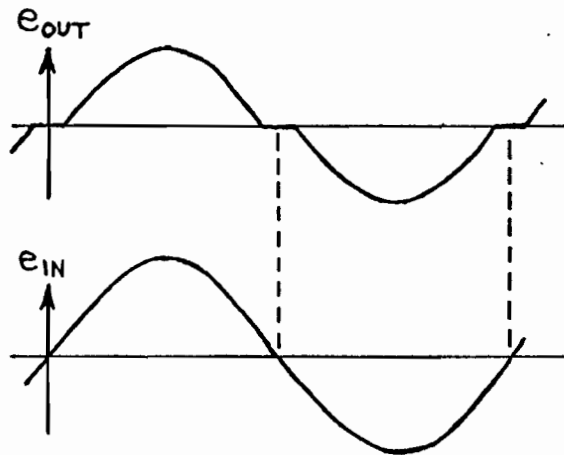


Figure 13. Distortion of Figure 12 circuit

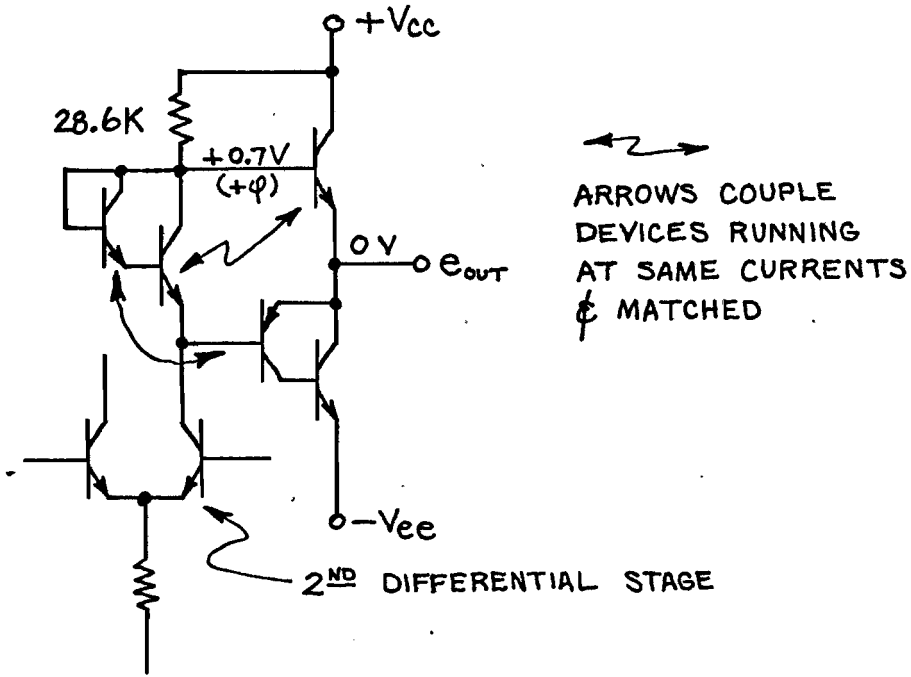


Figure 14. Transistor matching to reduce distortion

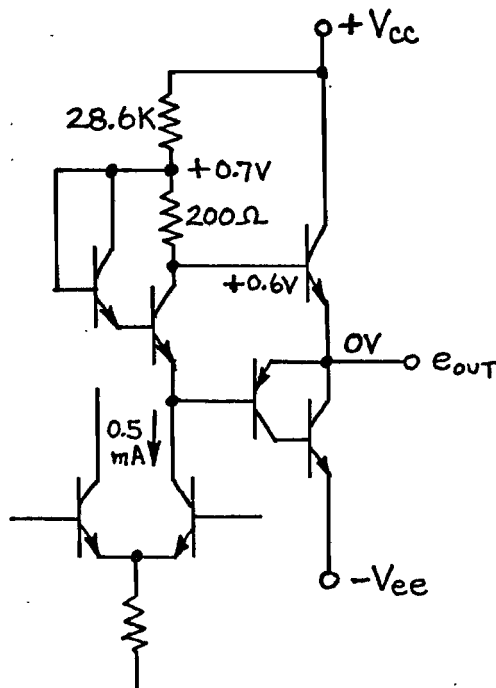


Figure 15. Resistive drop reduces current consumption

this still does not represent the ultimate output stage.

Figure 15 illustrates a technique which has been found to satisfy the simultaneous requirements of low distortion and low power consumption [10]. Transistor matching is used as in Figure 14, but a resistor is added to reduce consumption in the output stage. Since transistor current flow will decrease a factor of 10 for each 60 mV reduction in base emitter potential the voltage drop across the resistor can be used to adjust output stage quiescent current when $e_{OUT} = 0$. During positive swing, this drop and the current flow through the matching transistors will both decrease, tending to create matching drops and maintaining output quiescent current essentially constant. In a similar fashion, during negative swing, transistor and resistor drops will increase, maintaining constant quiescent current.

Short Circuit Protection

With a class B output stage, significant current flow can occur if the output is accidentally shorted to ground, and device destruction is the usual result. It would be desirable to have a circuit which would tolerate short circuits without burn-out.

Figure 16 shows how the addition of two transistors and two resistors to the basic circuit can protect the output stage from destructive current flow and power dissipation.

The 30 Ω resistors have been chosen so that the associated device will begin conduction at an output current of 20 mA at room temperature, thus robbing the output stage of base drive, and preventing high current flow.

It is interesting to note that since base-emitter threshold

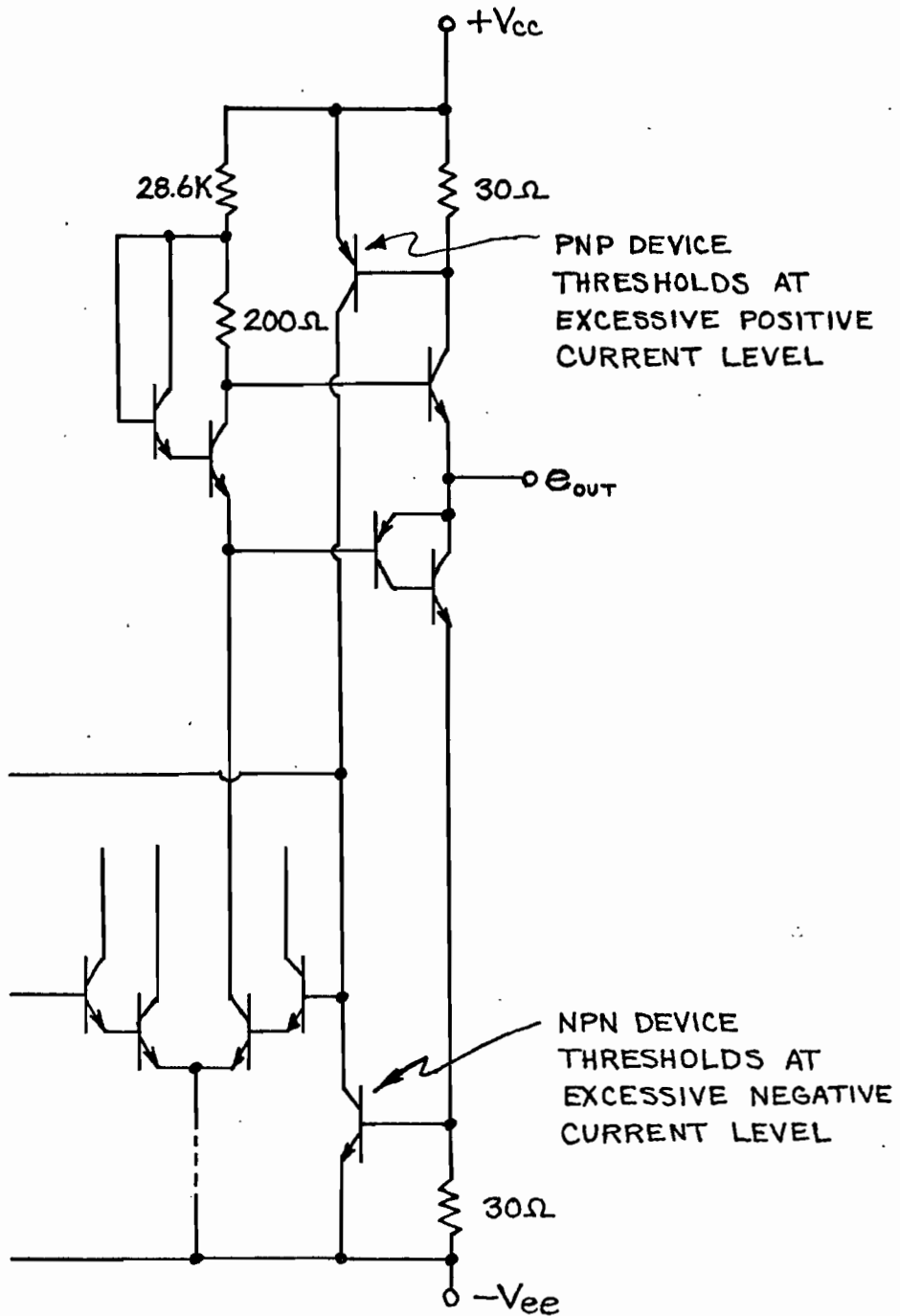


Figure 16. Short circuit protection devices

potentials decrease with temperature, current limiting will occur at 13 mA when the temperature is $+125^{\circ}\text{C}$, thus reducing short circuit dissipation when the device is already at an elevated temperature. At very low temperatures, when more dissipation can be tolerated, current limiting occurs at 27 mA.

CHAPTER V

EXPERIMENTAL RESULTS

Experimental Model

An experimental model was constructed according to the final schematic shown in Figure 17. The circuit was assembled using resistor values as close to the theoretical design as possible consistent with RETMA standard values. The NPN devices used were integrated five layer devices (p substrate, N+ buried layer, N epitaxial layer, P base diffusion, N+ emitter diffusion) so that experimental results obtained from the model would correlate well with expected performance from a future monolithic realization. The PNP devices used were lateral PNP's [1] constructed from the same diffusion schedule as the NPN's. The field-effect transistors were discrete devices but were of double-diffused construction which would be the type obtained with integrated circuit fabrication techniques. The electrical characteristics of the devices used were given during the circuit design portions of this paper.

Definition of Operational Amplifier Parameters

Before discussing the experimental results, it would be useful to define some important parameters of operational amplifiers so that the data obtained may be more easily understood. Parameter names, symbols, and definitions are given in Table I, and may be related to

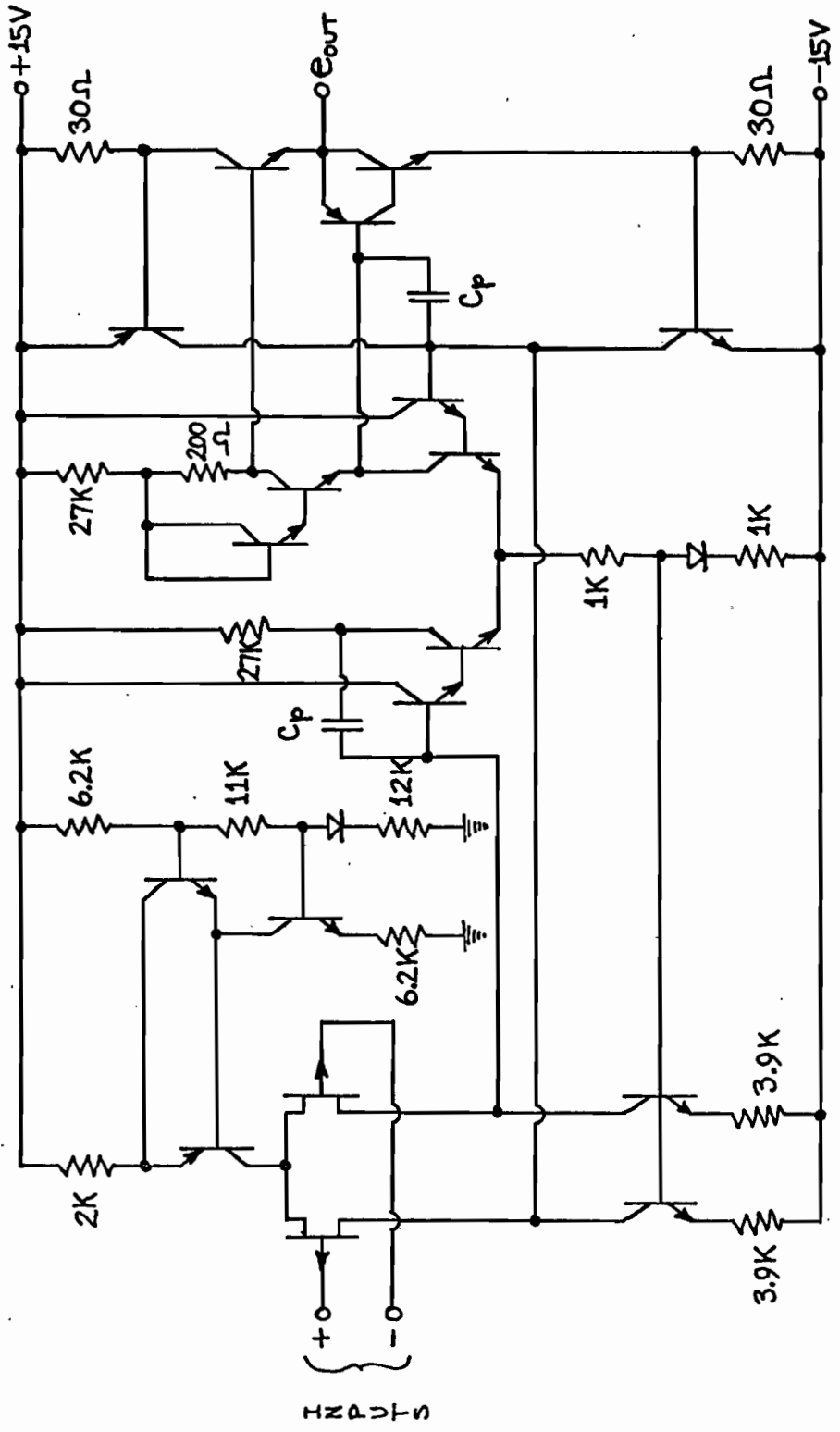


Figure 17. Final circuit diagram of experimental model

PARAMETER	SYMBOL	DEFINITION
Offset Voltage	V_{OS}	$V_1 - V_2$, when $V_{OUT} = 0$
Input Bias Current	I_B	$\frac{I_1 + I_2}{2}$, when $V_{OUT} = 0$
Offset Current	I_{OS}	$I_1 - I_2$, when $V_{OUT} = 0$
Offset Voltage Drift	$V_{OS} (T)$	$\frac{\Delta V_{OS}}{\Delta T}$, when $V_{OUT} = 0$
Input Bias Current Drift	$I_B (T)$	$\frac{\Delta I_B}{\Delta T}$, when $V_{OUT} = 0$
Offset Current Drift	$I_{OS} (T)$	$\frac{\Delta I_{OS}}{\Delta T}$, when $V_{OUT} = 0$
Positive Power Supply Rejection	PS_{REJ}^+	$\frac{\Delta V_{OUT}}{\Delta V_{cc} \cdot G_{OL}}$
Negative Power Supply Rejection	PS_{REJ}^-	$\frac{\Delta V_{OUT}}{\Delta V_{ee} \cdot G_{OL}}$
Open Loop Gain	G_{OL}	$\frac{\Delta V_{OUT}}{\Delta(V_1 - V_2)}$
Common Mode Rejection	CM_{REJ}	$\frac{\Delta V_{OUT}}{\Delta V \cdot G_{OL}}$, $V_1 = V_2 = V$
Maximum Input Common Mode Swing	$CMV_{IN,MAX}$	$V_1 = V_2 = V$, Max. + and - value of V with circuit active
Maximum Output Swing	$V_{OUT,MAX}$	Max. peak to peak output voltage without clipping
Slew Rate	S	$\frac{\Delta V_{OUT}}{\Delta t}$, input overdriven

TABLE I. DEFINITION OF OPERATIONAL AMPLIFIER PARAMETERS
(Refer to Figure 18)

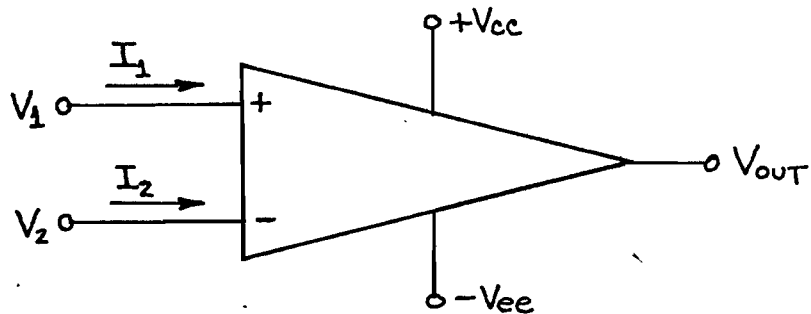


Figure 18. Operational amplifier block diagram

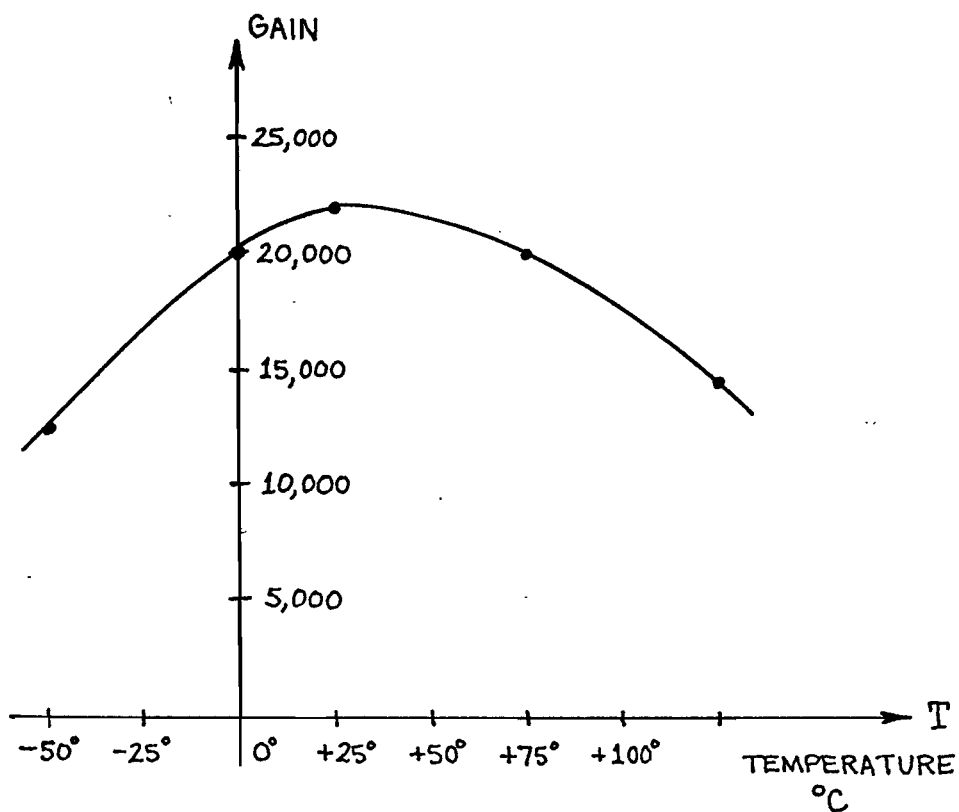


Figure 19. D.C. Gain versus temperature

the basic block diagram shown in Figure 18.

D.C. Characteristics

The D.C. characteristics obtained from the model are given in Table II. (I_{OS} and I_{OS} drift were not measured since the model was constructed with unmatched field-effect devices, and it was felt that data obtained on these parameters would not be valid.) In addition, a plot of D.C. gain versus temperature is shown in Figure 19. It is to be noted that measured gain at room temperature is very close to that calculated from the design sections.

High Frequency Characteristics

High frequency characteristics have been summarized in the plot of gain versus frequency in Figure 20. Curves are given for $C_p = 0$ (uncompensated), $C_p = 5$ pf, and $C_p = 10$ pf. With $C_p = 5$ pf, unity feedback was applied, and the amplifier was found to be stable. In this condition the amplifier would tolerate approximately 60 pf of load capacitance before oscillating. Phase margin was not measured due to noise masking the signal above 5 MC.

It is to be noted here that any compensation capacitor applied to an amplifier limits the maximum rate at which the output voltage can be changed, even under overdrive conditions. This maximum rate is called the "slew rate". Slew rate, S , is determined by capacitor size and current available to drive it:

$$S = \frac{I}{C} \quad (\text{volts/sec.}) \quad (28)$$

In this particular case, $I = 0.25$ mA, and $C_p = 5$ pf; thus $S = 50$ V/ μ sec. Experimentally, the circuit measured exactly this

PARAMETER	MEASURED VALUE	COMMENTS
V_{OS}	89 mV	Unmatched input devices
I_B	0.8 nA	
I_{OS}	--	See text
$V_{OS} (T)$	60 $\mu\text{V}/^\circ\text{C}$	Unmatched input devices
$I_B (T)$	--	See text
$I_{OS} (T)$	--	See text
PS_{REJ}^+	8 $\mu\text{V}/\text{V}$	Ratios off with RETMA values, IC will be better
PS_{REJ}^-	Not measurable	
G_{OL}	22,000 @ 25 $^\circ\text{C}$	Close to theoretical calculation
CM_{REJ}	- 92 db	
$CMV_{IN, MAX}$	+ 13 V, - 10V	
$V_{OUT, MAX}$	22 V P-P into 1 K	

TABLE II. EXPERIMENTAL D.C. CHARACTERISTICS

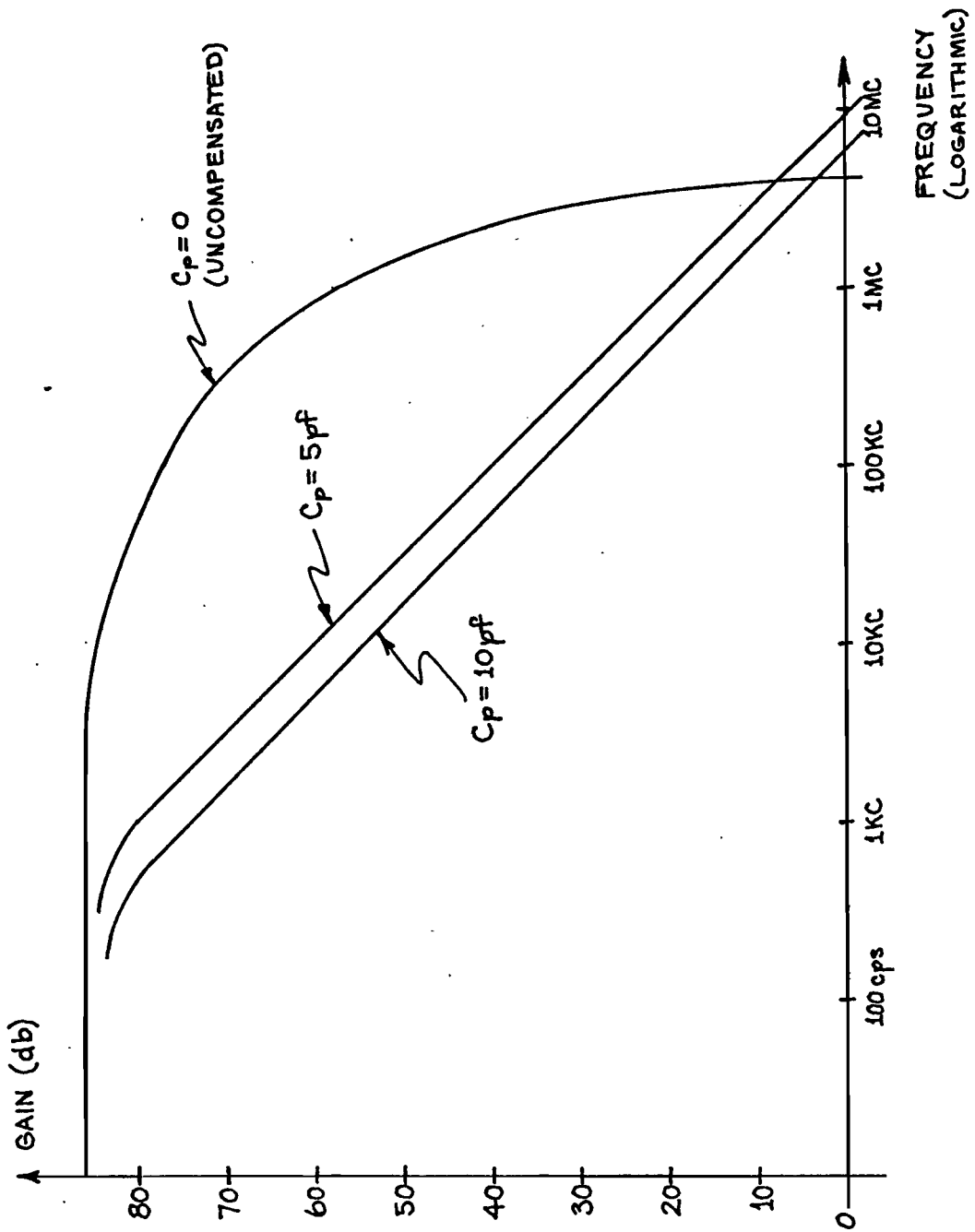


Figure 20. Gain versus frequency

value.

Class B Stage and Short Circuit Protection

The output stage power capability was measured and was found adequate to provide a low distortion 22 V P-P swing into a 1 K load.

The short circuit protection circuitry was found to limit at 22 mA from the positive supply and 20 mA from the negative supply.

Discussion of Experimental Results

The characteristics measured here compare quite favorably with present integrated circuit operational amplifiers. Input current is two orders of magnitude smaller than that obtained from conventional circuits. Usable gain-bandwidth product and slew rate are both approximately five times better than normally obtained.

CHAPTER VI

MONOLITHIC REALIZATIONDevices

All the transistors in this circuit design, except for the field-effect input devices, have been fabricated on a single monolithic chip before and have exhibited matching and tracking of characteristics to a degree unattainable with discrete devices.

Methods have been devised for fabricating junction field-effect devices on the same monolithic chip with NPN and lateral PNP devices [11]. These approaches usually add one additional diffusion step to normal processing methods to produce a high quality, high breakdown voltage, field-effect device. Figure 21 outlines the basic processing steps in fabricating a field-effect device which is compatible with present processing methods.

Resistors

Resistors are formed from transistor base diffusions as was shown in Figure 21. While absolute tolerance control of resistor values may be as large as $\pm 30\%$, ratios of resistors can be controlled to better than $\pm 2\%$.

Since resistors are formed from material with sheet resistivity near $200 \Omega/\square$, resistors of large value take up much surface area on a monolithic chip. Therefore, it is wise to limit total resistance

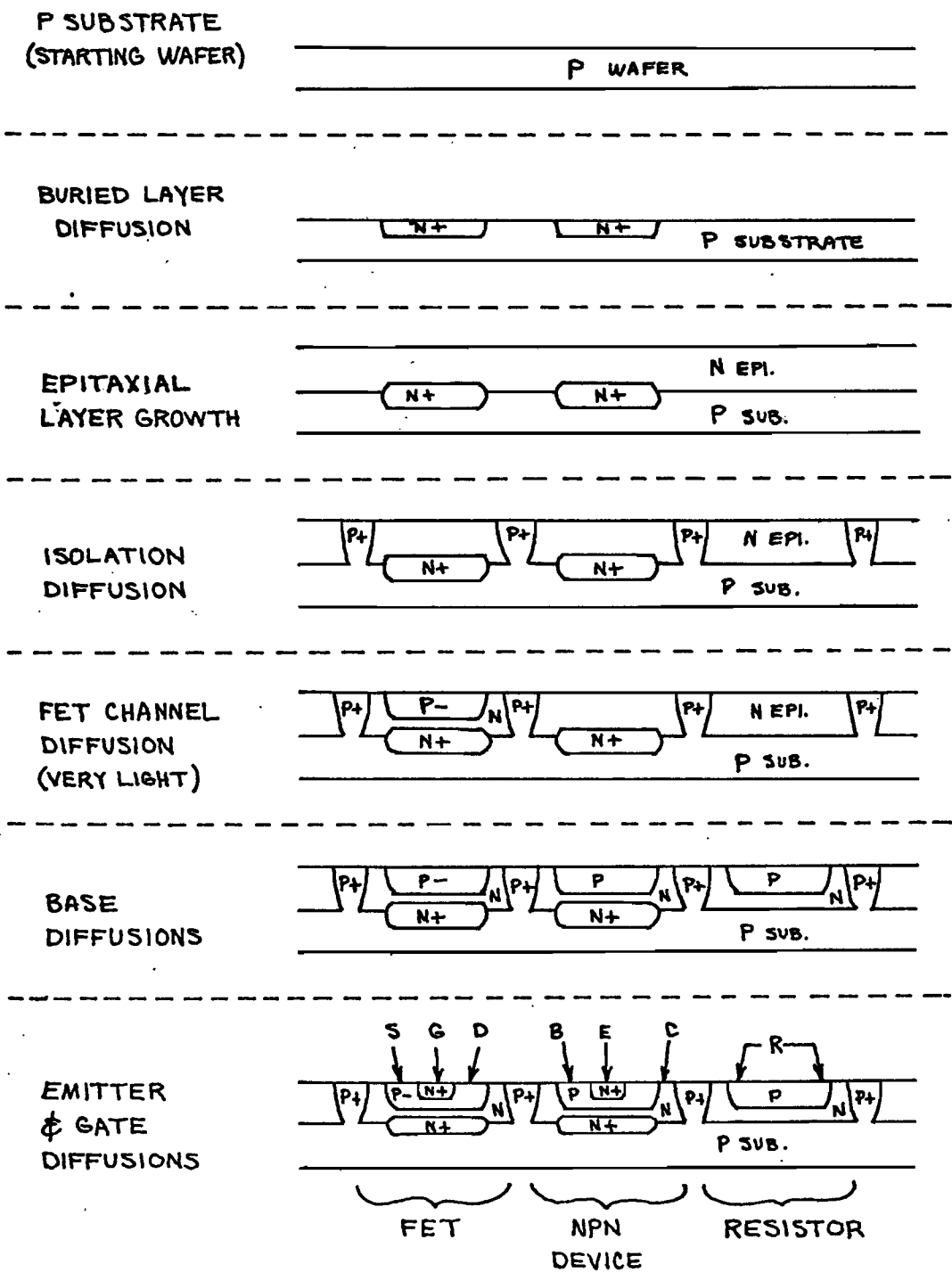


Figure 21. Monolithic processing steps

to < 100 K to keep chip size reasonable (e.g. 60 mil x 60 mil). For this amplifier total resistance is approximately 103 K.

Monolithic Improvements

Since transistor characteristics are matched, and resistor ratios are within $\pm 2\%$, we can expect that the monolithic realization will perform better than discrete in a number of ways.

Because the common mode analysis gave resistor ratio restraints, we may expect power supply rejection and common rejection to be improved over the measurements attained with the experimental model.

With matched monolithic devices, on one small piece of essentially isothermal silicon, offset voltages and currents and associated drift rates may be expected to improve.

In addition, since we can process the field-effect device to yield optimum performance for this particular circuit configuration, we may expect a gain improvement to at least a value of 10^5 (100 db), which will place the performance of this monolithic operational amplifier above all other contemporary monolithic units.

CHAPTER VII

SUMMARY

The circuit design of an operational amplifier configuration, utilizing field-effect input devices compatible with integrated circuit fabrication techniques, has been described.

The circuit has been shown to exhibit electrical characteristics which far surpass the capabilities of contemporary monolithic integrated circuit operational amplifiers.

Basic processing methods required for monolithic realization of the amplifier have been described, and circuit performance improvements due to integrated circuit characteristics have been shown.

This circuit in integrated form is expected to compete favorably with very expensive, special purpose, discrete component operational amplifiers.

BIBLIOGRAPHY

BIBLIOGRAPHY

- [1] H. C. Lin, T. B. Tan, G. Y. Chang, B. van der Leest, and N. Formigoni, "Lateral Complementary Transistor Structure for the Simultaneous Fabrication of Functional Blocks", Proc. IEEE, Vol. 52, No. 12, December, 1964; pp. 1491-1495.
- [2] J. E. Solomon and T. M. Frederiksen, "Monolithic Integrated Circuits", IEEE International Convention Record, 1967, to be published.
- [3] R. D. Middlebrook, Differential Amplifiers, John Wiley and Sons, Inc., New York and London, 1963; pp. 16-18.
- [4] Ibid., pp. 53-54
- [5] U. L. Rohde, "The Field-effect Transistor at V. H. F.", Wireless World, Vol. 72, No. 1, January, 1966, pp. 2-6.
- [6] R. D. Thornton, et al, Multistage Transistor Circuits, SEEC/ Vol. 5, John Wiley and Sons, Inc., New York, 1965; p. 5.
- [7] J. E. Solomon, "Lecture 7, Linear Integrated Circuits", University of California Statewide Lecture Series, Winter 1967; pp. 22-23, to be published, 1967.
- [8] R. D. Thornton, et al, *op. cit.*; pp. 18-19.
- [9] J. E. Solomon and G. R. Wilson, "A highly Desensitized, Wide-Band Monolithic Amplifier", IEEE Journal of Solid-State Circuits, Vol. SC-1, No. 1, September, 1966; pp 19-28.
- [10] M. J. Gay, Allen Clark Research Centre, Plessey Co., Ltd., Northants, England; private communication.
- [11] R. M. Warner, Jr., and J. N. Fordemwalt, editors, Integrated Circuits, Design Principles and Fabrication, McGraw-Hill Book Co., New York, 1965; Chapter 8, pp. 208-218.

BIOGRAPHICAL SKETCH

James Elbert Thompson was born in Washington, D. C. on February 29, 1940. He received his elementary and secondary education in the public schools of Huntington, West Virginia. In 1958 he entered the Massachusetts Institute of Technology on an Alumni Fund National Scholarship and graduated in 1962, receiving the Bachelor of Science degree in Electrical Engineering. Since June, 1962, he has been employed by Motorola Semiconductor Products Division. He is presently Section Manager, Linear Integrated Circuits Research and Development, specializing in Automotive, Industrial, and Appliance Controls. He has studied for the degree of Master of Science in Engineering on a part-time basis since September 1962. He is married and the father of two children.