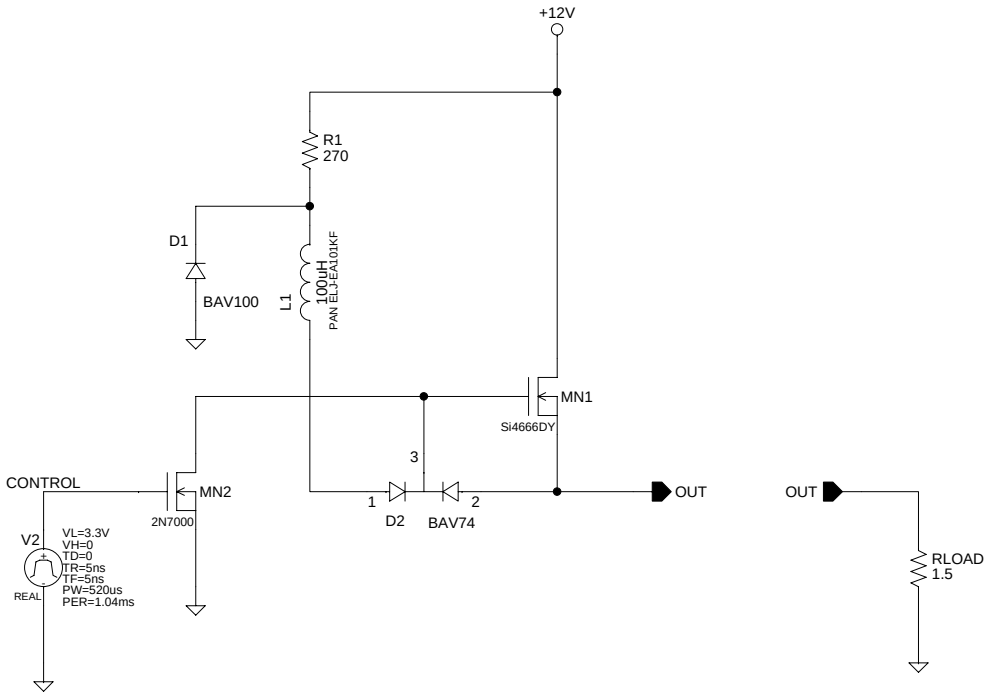


LIBRARY: C:\PSpice\SpiceModels\PowerMOSFET\supertex.lib

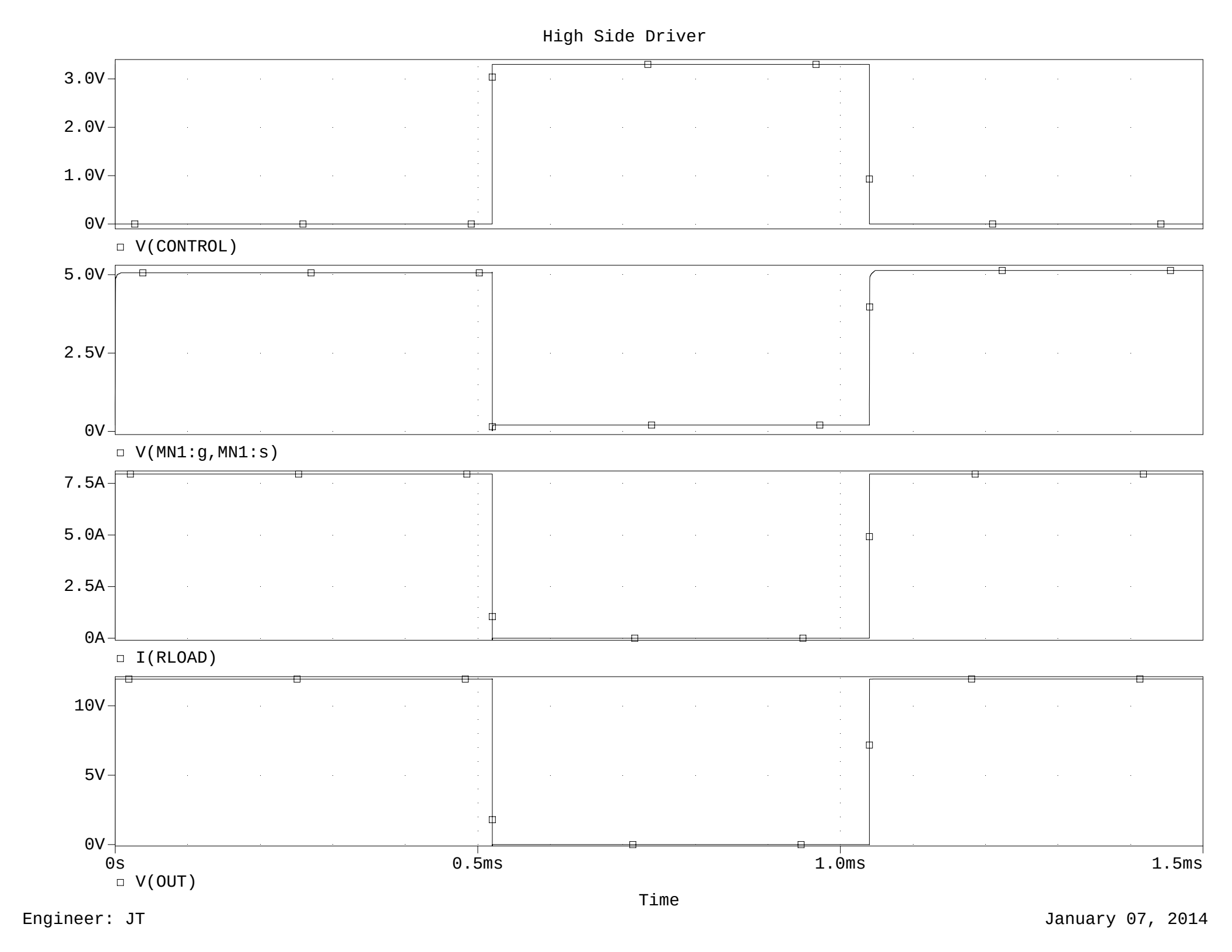
LIBRARY: C:\PSpice\DeviceLib\Vishay\Si4666DY_PS.lib

ANALOG INNOVATIONS
35129 N LAREDO DR
SAN TAN VALLEY, AZ 85142-3361
(480) 460-2350 FAX: (602) 557-0890

Title:
High Side Driver from 3.3V Logic

Size	FileName:	REV
A	C:\Projects\Expments\SED\HighSideDriver.sch	A

January 7, 2014, 9:38 AM	Sheet 1 of 1


High Side Driver
3.0V
2.0V
1.0V
0V
V(CONTROL)
5.0V
2.5V
0V
V(MN1:g,MN1:s)
7.5A
5.0A
2.5A
0A
I(RLOAD)
10V
5V
0V
0s
0.5ms
1.0ms
1.5ms
V(OUT)
Time
Engineer: JT
January 07, 2014

```
* C:\Projects\Expments\SED\HighSideDriver.sch

* Schematics Version 15.7.0
* Tue Jan 07 09:29:00 2014

** Analysis setup **
.tran 1.5m 1.5m 0 100n
.OPTIONS STEPGMIN
.OP

X_L1          N_1 N_2 L_PARAM PARAMS: L=100uH RS=2.4 SRF=8Meg
D_D1          0 N_2 BAV100
***          RealPulse ***
          R1V2 $N1V2 0 1K
          R2V2 $N2V2 0 1K
          E1V2 $N2V2 0 VALUE {1.570796*SIN(V($N1V2,0))}
          V1V2 $N1V2 0 PULSE -1.570796 1.570796
          {LIMIT((0-1.25*5ns),0,1E6)}
+ {2.5*5ns} {2.5*5ns} {520us-2.5*5ns} 1.04ms
          E2V2 CONTROL 0 VALUE {(0-3.3V)/2*SIN(V($N2V2,0))+(0+3.3V)/2}
                  *******
X_D2          N_1 OUT N_3 BAV74
V_V1          N_4 0 +12V
R_RLOAD          OUT 0  1.5
X_MN1          N_4 N_3 OUT Si4666DY
R_R1          N_4 N_2  270
MN_MN2          N_3 CONTROL 0 0 2N7000

***
.SUBCKT DMG1012T 10 20 30   ; D, G, S
*     TERMINALS:  D  G  S
M1   1  20  3  3  NMOS L=0.6U W=47.66m
RD  10  1  220m
RS  30  3  80m
CGS  20  3  57p
EGD 12  0  20  1  1
VFB 14  0  0
FFB  20  1  VFB  1
CGD 13 14  27p
R1  13  0  1.00
D1  12 13  DLIM
DDG 15 14  DCGD
R2  12 15  1.00
D2  15  0  DLIM
DSD  3 10  DSUB
.MODEL NMOS NMOS LEVEL=3 U0=500 VMAX=80k
+ ETA=0.1m VTO=0.99 TOX=16.8n NSUB=4.57e16
.MODEL DCGD D CJO=27p VJ=80m M=0.320
.MODEL DSUB D IS=36.1n N=1.50 RS=21.8m BV=20
+ CJO=14p VJ=0.800 M=0.420
.MODEL DLIM D IS=100U
```

```
.ENDS
***
.SUBCKT  Si4666DY D G S
M1 3 GX S S NMOS W= 1991950u L= 0.25u
M2 S GX S D PMOS W= 1991950u L= 3.932e-07
R1 D 3 6.827e-03 TC=4.617e-03 8.468e-06
CGS GX S 8.371e-10
CGD GX D 2.356e-11
RG G GY 0.6
RTCV 100 S 1e6 TC=-8.905e-05 -7.009e-07
ETCV GX GY 100 200 1
ITCV S 100 1u
VTCV 200 S 1
DBD S D DBD
**********************************************************
.MODEL NMOS NMOS ( LEVEL = 3 TOX = 5e-8
+ RS = 6.651e-04 KP = 2.155e-05 NSUB = 3.394e+16
+ KAPPA = 1.000e-06 ETA = 5.949e-07 NFS = 4.098e+11
+ LD = 0 IS = 0 TPG = 1)
**********************************************************
.MODEL PMOS PMOS ( LEVEL = 3 TOX = 5e-8
+NSUB = 1.519e+16 IS = 0 TPG = -1 )
**********************************************************
.MODEL DBD D (
+FC = 0.1 TT = 7.238e-09 T_MEASURED = 25 BV = 26
+RS = 1.034e-02 N = 1.015e+00 IS = 9.509e-11
+EG = 8.714e-01 XTI = 2.937e+00 TRS1 = 1.000e-05
+CJO = 4.801e-10 VJ = 6.322e-01 M = 3.984e-01 )
.ENDS
***
.MODEL 2N7000   NMOS (LEVEL=3   RS=0.205          NSUB=1.0E15
+DELTA=0.1      KAPPA=0.0506    TPG=1            CGDO=3.1716E-9
+RD=0.239       VTO=1.000       VMAX=1.0E7       ETA=0.0223089
+NFS=6.6E10     TOX=1.0E-7      LD=1.698E-9      UO=862.425
+XJ=6.4666E-7   THETA=1.0E-5    CGSO=9.09E-9     L=2.5E-6
+W=0.8E-2)
**********************************************************
.SUBCKT L_PARAM 1 2 PARAMS: L=100uH RS=2.4 SRF=8E6
L 1 3 {L}
RS 3 2 {RS}
CS 1 2 {1/(2*pi*SRF)/(2*pi*SRF)/L}
.ENDS L_PARAM
**********************************************************
.SUBCKT BAV74 1 2 3
D1 1 3 DBAV74
D2 2 3 DBAV74
.model DBAV74    D(Is=1.211n N=1.797 Rs=.8837 Ikf=0 Xti=3 Eg=1.11
Cjo=2p M=.3333
+               Vj=.5 Fc=.5 Isr=21.22n Nr=2 Tt=5.771n)
*   SIEMENS   pid=bav74 case=SOT23
*   91-08-29 dsq
```

```
* Changed to dual diodes (one package) RAP 5-28-96
.ENDS
***
.model BAV100  D(Is=546.9n N=2.854 Rs=.1647 Ikf=.1486 Xti=3 Eg=1.11
Cjo=1.456p
+                M=.3333 Vj=.5 Fc=.5 Bv=60 Ibv=100u Tt=72.13n)
*   PHILIPS   pid=bav103  case=SOD80
*   91-08-20 dsq
***
.END
```