

## CIRCUIT 1 – Explanation of Operation

Figure 1 is the schematic of Circuit1, as originally posted.

I thought it was obvious, but maybe not, but this is a pair of cascaded CMOS inverters, with some extra CMOS devices thrown in.

The best way to go about analyzing a circuit of this sort is to assume a logical state and see what results.

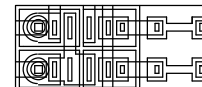
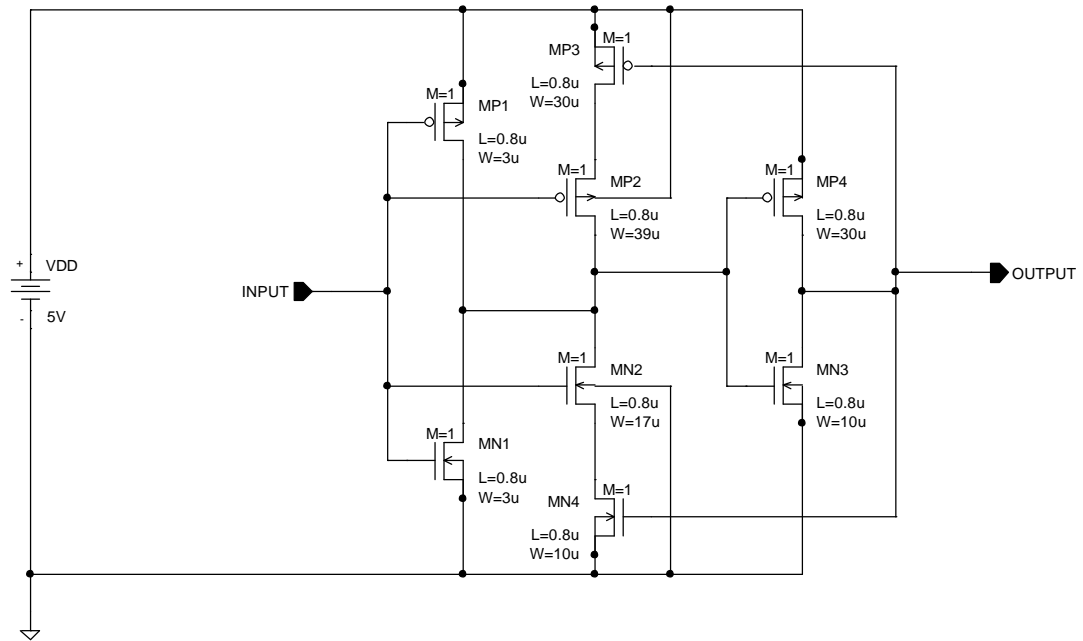
For example, if we assume the input is a logical “LOW”, then MP1 and MP2 are definitely in an “ON” state and MN1 and MN2 are “OFF”. We note that we don’t really care what MP3 and MN4 are doing, the gates of MP4 and MN3 are definitely a “HIGH”, so the output is “LOW”. Thus MN4 is “OFF” and MP3 is “ON”. This reduction is shown in Figure 2A. Paralleled devices with the same “L” value can be merged by adding the widths (“W”). This reduction is shown in Figure 2B.

Studying Figure 2B we see a very large (strong) P-channel device, MP1+2, opposing a small (weak) N-channel device, MN1. So we would conclude that the input would need to go quite high before strength balance between MP1+2 and MN1 would be achieved and the output state would change to a “HIGH”.

Now assume a starting state of input “HIGH”, MN1 and MN2 are definitely in an “ON” state and MP1 and MP2 are “OFF”, so the output state must also be “HIGH”, as shown in Figure 3A. Combining paralleled devices, as before, by adding widths, we arrive at Figure 3B.

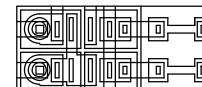
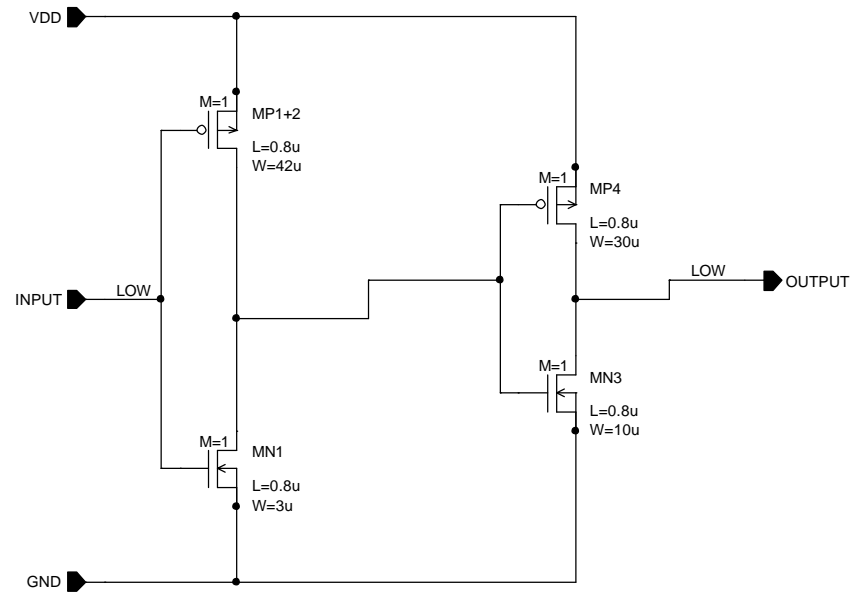
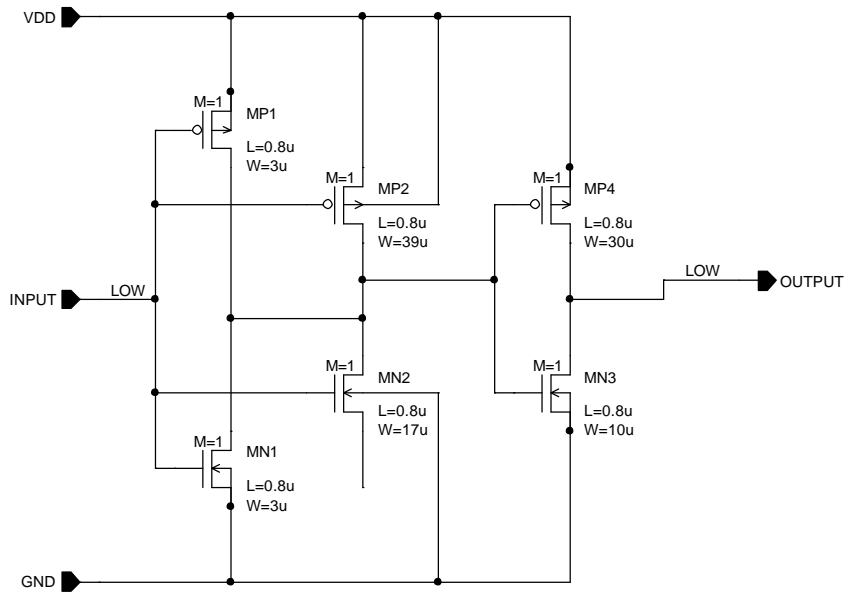
In Figure 3B we have just the opposite case as in Figure 2B, the combined N-channel device MN1+2 is much stronger than P-channel device MP1. So we would conclude that the input would need to go quite low before strength balance between MP1 and MN1+2 would be achieved and the output state would change to a “LOW”.

Hmmmm! These required logic states, for change to occur, would seem to imply hysteresis. What we have here is a buffer with hysteresis, with simulation results as shown in Figure 4.



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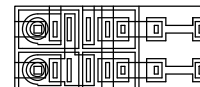
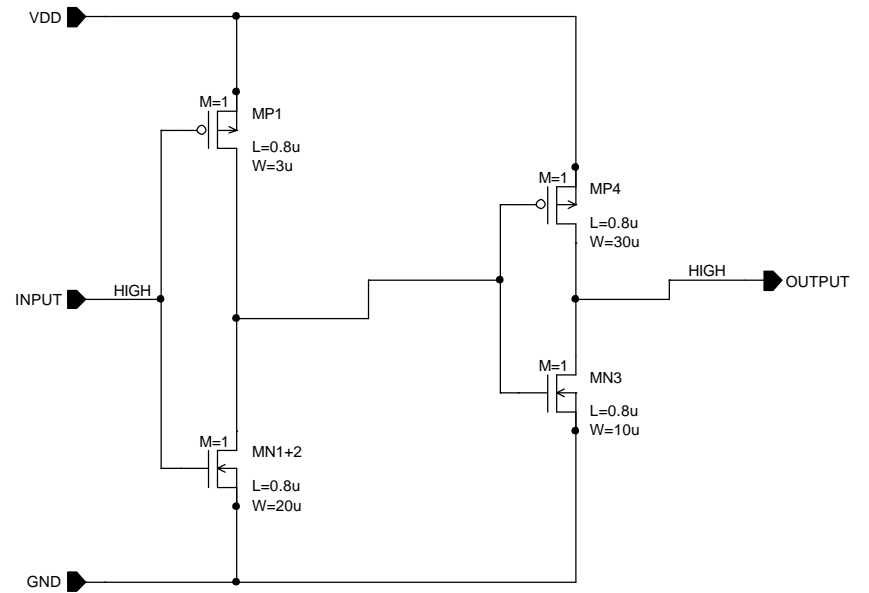
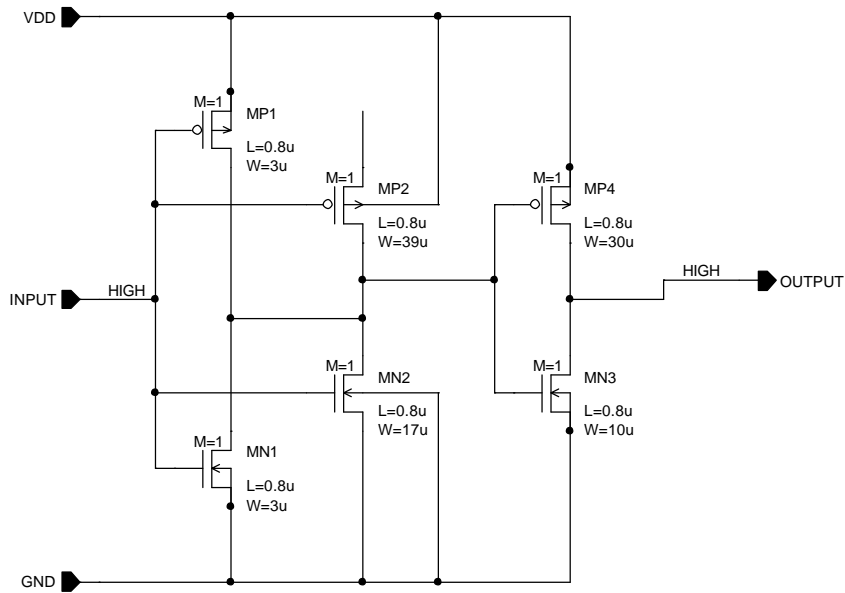
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Title:  
Circuit 1 - Input Low

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November 9, 2005, 3:39 PM		Sheet 1 of 1



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Title:  
Circuit 1 - Input High

Size A	FileName: D:\Projects\Expments\SED\Contest1\Circuit1-High.sch	REV A
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Sheet 1 of 2

Circuit1...Hysteresis

