



# Phase-Frequency Detector

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648, MC12147, MC12148 or MC12149), it is useful in a broad range of phase-locked loop applications.

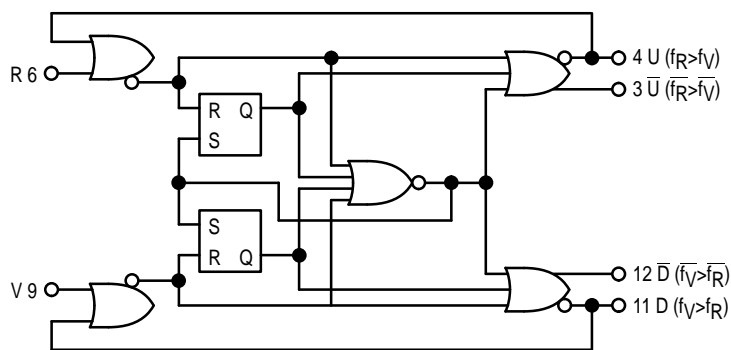
- Operating Frequency = 80 MHz Typical

## Pin Conversion Table

14 PIN DIP	1	2	3	4	5	6	7	8	9	10	11	12	13	14
20 PIN PLCC	2	3	4	6	8	9	10	12	13	14	16	18	19	20

Inputs		Outputs			
R	V	U	D	$\bar{U}$	$\bar{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

## LOGIC DIAGRAM



$V_{CC1}$  = Pin 1  
 $V_{CC2}$  = Pin 14  
 $V_{EE}$  = Pin 7

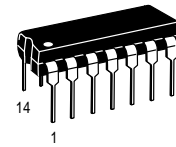
## TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

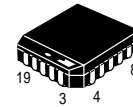
# MC12040

## PHASE-FREQUENCY DETECTOR

### SEMICONDUCTOR TECHNICAL DATA



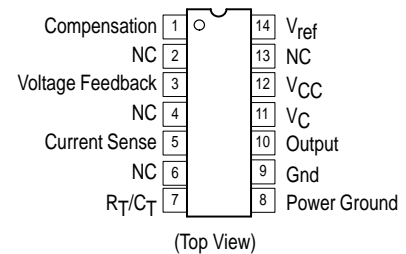
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646



**FN SUFFIX**  
PLASTIC PACKAGE  
CASE 775  
(PLCC)

*Not Recommended for New Designs*

## PIN CONNECTIONS



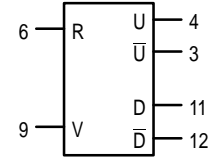
## ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC12040P	$T_A = 0^\circ$ to $+75^\circ\text{C}$	Plastic

# MC12040

## ELECTRICAL CHARACTERISTICS

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



**NOTE:** For more information on using an ECL device in a +5V system, refer to Motorola Application Note AN1406/D, "Designing with PECL (ECL at +5.0V)"

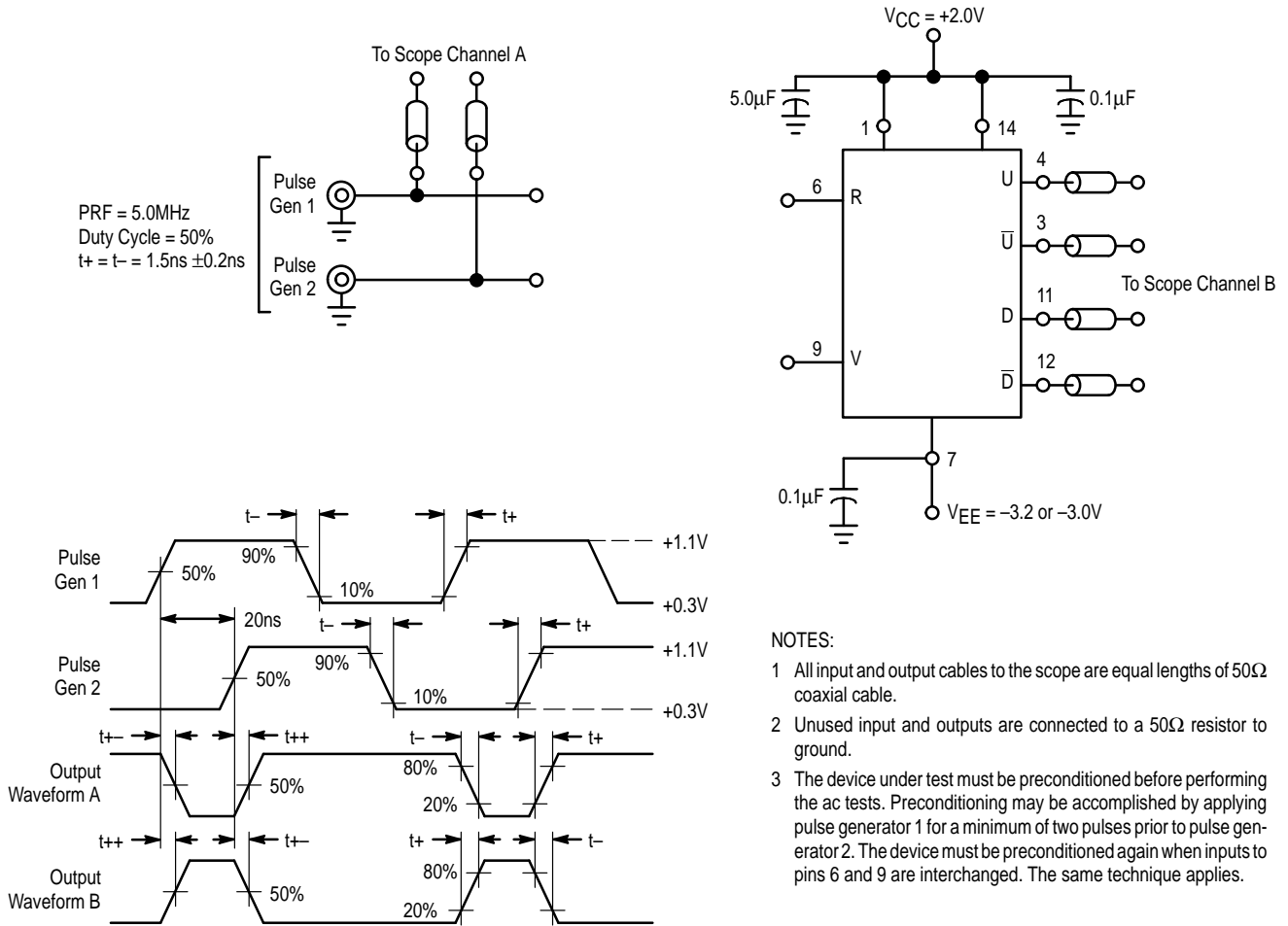
		TEST VOLTAGE VALUES														
		(Volts)														
		@ Test Temperature														
		V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>EE</sub>										
		0°C	-0.840	-1.870	-1.145	-1.490	-5.2									
		25°C	-0.810	-1.850	-1.105	-1.475	-5.2									
		75°C	-0.720	-1.830	-1.045	-1.450	-5.2									
		TEST VOLTAGE APPLIED TO PINS BELOW														
		(V <sub>CC</sub> ) Gnd														
		MC12040														
		0°C		25°C		75°C		Unit		TEST VOLTAGE APPLIED TO PINS BELOW						
Symbol	Characteristics	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>EE</sub>		
I <sub>E</sub>	Power Supply Drain	7			-120	-60			mAdc					7	1,14	
I <sub>INH</sub>	Input Current	6 9				350 350			μAdc	6 9				7 7	1,14 1,14	
V <sub>OH</sub> <sup>1</sup>	Logic "1" Output Voltage	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc					7	1,14	
V <sub>OL</sub> <sup>1</sup>	Logic "0" Output Voltage	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc					7	1,14	
V <sub>OHA</sub> <sup>2</sup>	Logic "1" Input Voltage	3 4 11 12	-1.020		-0.980		-0.920		Vdc			6.9		7	1,14	
V <sub>OLA</sub> <sup>2</sup>	Logic "0" Input Voltage	3 4 11 12		-1.615		-1.600		-1.575	Vdc			9 6 9 6	6 9 6 9	7	1,14	

Supply Voltage = +5.0V

		TEST VOLTAGE VALUES														
		(Volts)														
		@ Test Temperature														
		V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>EE</sub>										
		0°C	+4.160	+3.130	+3.855	+3.510	+5.0									
		25°C	+4.190	+3.150	+3.895	+3.525	+5.0									
		75°C	+4.280	+3.170	+3.955	+3.550	+5.0									
		TEST VOLTAGE APPLIED TO PINS BELOW														
		(V <sub>CC</sub> ) Gnd														
		MC12040														
		0°C		25°C		75°C		Unit		TEST VOLTAGE APPLIED TO PINS BELOW						
Symbol	Characteristics	Pin Under Test	Min	Max	Min	Max	Min	Max	Unit	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmx</sub>	V <sub>EE</sub>		
I <sub>E</sub>	Power Supply Drain	7			-115	-60			mAdc					1,14	7	
I <sub>INH</sub>	Input Current	6 9				350 350			μAdc	6 9				1,14 1,14	7 7	
V <sub>OH</sub> <sup>1</sup>	Logic "1" Output Voltage	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7	
V <sub>OL</sub> <sup>1</sup>	Logic "0" Output Voltage	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7	
V <sub>OHA</sub> <sup>2</sup>	Logic "1" Input Voltage	3 4 11 12	3.980		4.020		4.080		Vdc			6.9		1,14	7	
V <sub>OLA</sub> <sup>2</sup>	Logic "0" Input Voltage	3 4 11 12		3.450		3.460		3.490	Vdc			9 6 9 6	6 9 6 9	1,14	7	

# MC12040

Figure 1. AC Tests



Symbol	Characteristic	Pin Under Test	Output Waveform	MC12040			Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED			
				0°C	25°C	85°C		Pulse Gen 1	Pulse Gen 2	V <sub>EE</sub> -3.0 or -3.2V	V <sub>CC</sub> +2.0V
				Max	Max	Max					
$t_{6+4+}$ $t_{6+12+}$ $t_{6+3-}$ $t_{6+11-}$ $t_{9+11+}$ $t_{9+3+}$ $t_{9+12-}$ $t_{9+4-}$	Propagation Delay	6,4 6,12 6,3 6,11 9,11 9,3 9,12 9,4	B A A B B A A B	4.6 6.0 4.5 6.4 4.6 6.0 4.5 6.4	4.6 6.0 4.5 6.4 4.6 6.0 4.5 6.4	5.0 6.6 4.9 7.0 5.0 6.6 4.9 7.0	ns	6 9 6 9 9 6 9 6	9 6 9 6 6 9 6 9	7	1,14
$t_{3+}$ $t_{4+}$ $t_{11+}$ $t_{14+}$	Output Rise Time	3 4 11 14	A B B A	3.4	3.4	3.8	ns	6 6 9 9	9 9 6 6	7	1,14
$t_{3-}$ $t_{4-}$ $t_{11-}$ $t_{14-}$	Output Fall Time	3 4 11 14	A B B A	3.4	3.4	3.8	ns	6 6 9 9	9 9 6 6	7	1,14

# MC12040

## APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 2), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 2), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle—that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage controlled oscillator can be developed. A circuit useful for this function is shown in Figure 3.

Proper level shifting is accomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector (U and D). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The U and D outputs are then used to pass along phase information to the operational amplifier. Phase summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (NO TAG) may be very beneficial since the very narrow correctional pulses of the MC12040 would not normally be integrated by the amplifier. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplifier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16mV offset voltage in the amplifier would cause an error of  $0.016 / 0.16 = 0.1$  radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 3). Phase error over temperature depends on how much the offending parameters drift.

Figure 2. Timing Diagram

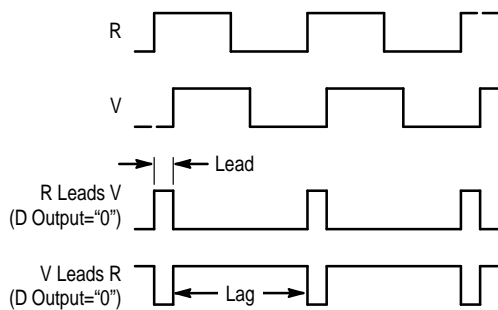
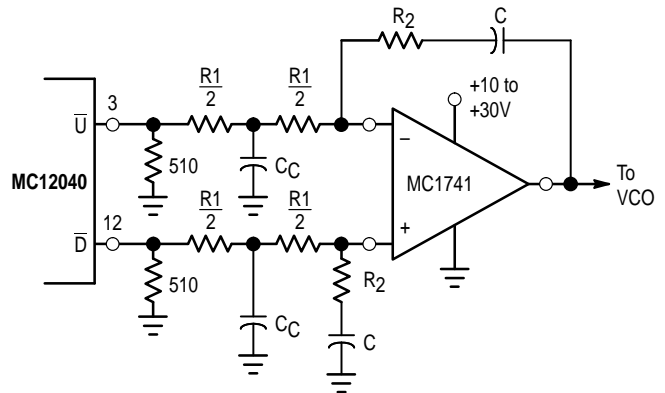


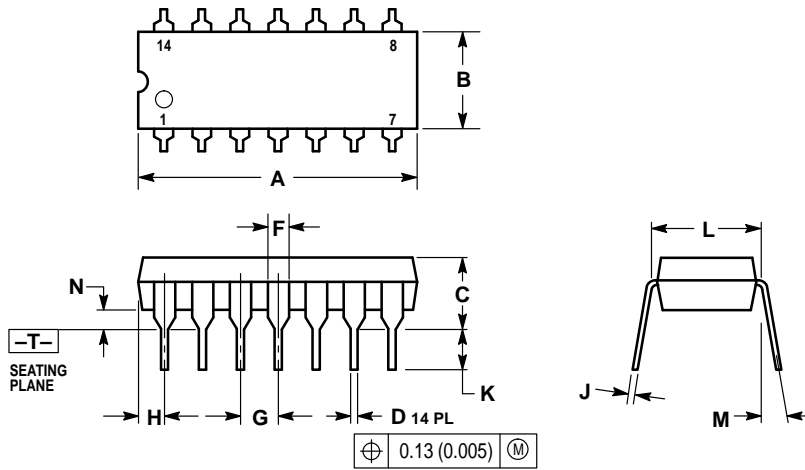
Figure 3. Typical Filter and Summing Network



# MC12040

## OUTLINE DIMENSIONS

P SUFFIX  
PLASTIC PACKAGE  
CASE 646-06  
ISSUE M



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	— 10°		— 10°	
N	0.015	0.039	0.38	1.01

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

**How to reach us:**

**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141,  
4-32-1 Nishi-Gotanda, Shagawa-ku, Tokyo, Japan. 03-5487-8488

**Customer Focus Center: 1-800-521-6274**

**Mfax™:** RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609  
Motorola Fax Back System – US & Canada ONLY 1-800-774-1848  
– http://sps.motorola.com/mfax/

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

**HOME PAGE:** <http://motorola.com/sps/>

