

Differential Video Amplifier

The MC1733CB is a wideband amplifier with differential input and differential output. Gain is fixed at 10 V, 100 V, or 400 V without external components. With the addition of one external resistor, gain becomes adjustable from 10 V to 400 V.

- Bandwidth: 120 MHz Typical @ $A_{VD} = 10$
- Rise Time: 2.5 ns Typical @ $A_{VD} = 10$
- Propagation Delay Time: 3.6 ns Typical @ $A_{VD} = 10$

Figure 1. Basic Circuit

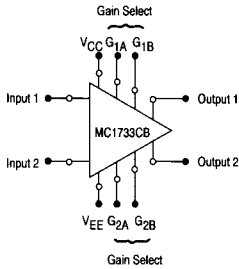


Figure 2. Voltage Gain Adjust Circuit

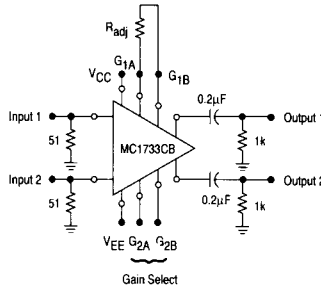
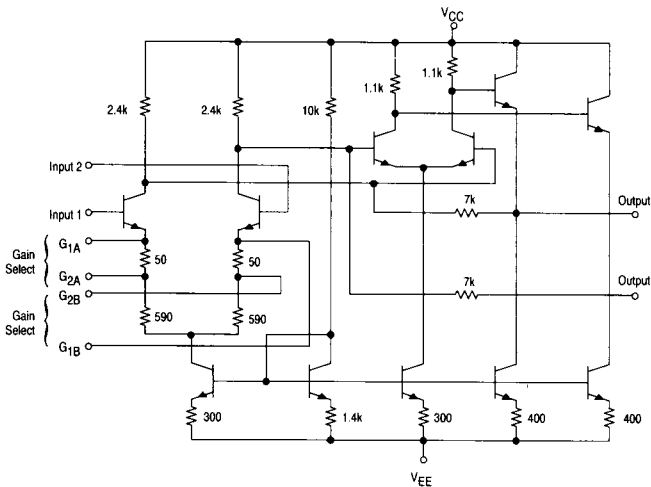


Figure 3. Equivalent Circuit Schematic



MC1733CB

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

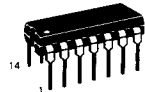
D SUFFIX
 PLASTIC PACKAGE
 CASE 751A
 (SO-14)



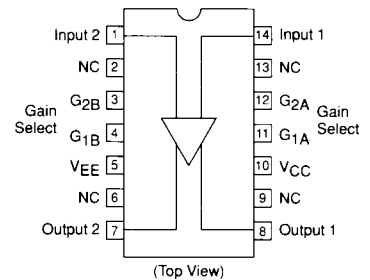
L SUFFIX
 CERAMIC PACKAGE
 CASE 632



P SUFFIX
 PLASTIC PACKAGE
 CASE 646



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1733CBD	0° to +70°C	SO-14
MC1733CBL		Plastic DIP
MC1733CBP		Ceramic DIP

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MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	+8.0	V
	V _{EE}	-8.0	V
Differential Input Voltage	V _{in}	±5.0	V
Common Mode Input Voltage	V _{ICM}	±6.0	V
Output Current	I _O	10	mA
Internal Power Dissipation	P _D	500	mW
Operating Temperature Range	T _A	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, @ +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit	
Differential Voltage Gain	A _{vd}	250	400	600	V/V	
						Gain 1 (Note 2)
						Gain 2 (Note 3)
						Gain 3 (Note 4)
Bandwidth (R _S = 50 Ω)	BW	—	40	—	MHz	
						Gain 1
						Gain 2
						Gain 3
Rise Time (R _S = 50 Ω, V _O = 1.0 V _{p-p})	t _{TLH} t _{THL}	—	10.5	—	ns	
						Gain 1
						Gain 2
						Gain 3
Propagation Delay (R _S = 50 Ω, V _O = 1.0 V _{p-p})	t _{PLH} t _{PHL}	—	7.5	—	ns	
						Gain 1
						Gain 2
						Gain 3
Input Resistance	R _{in}	—	4.0	—	kΩ	
						Gain 1
						Gain 2
						Gain 3
Input Capacitance (Gain 2)	C _{in}	—	2.0	—	pF	
Input Offset Current (Gain 3)	I _{IO}	—	0.4	5.0	μA	
Input Bias Current (Gain 3)	I _B	—	9.0	30	μA	
Input Noise Voltage (R _S = 50 Ω, BW = 1.0 kHz to 10 MHz)	V _n	—	12	—	μV(rms)	
Input Voltage Range (Gain 2)	V _{in}	±1.0	—	—	V	
Common Mode Rejection	CMR	60	86	—	dB	
						Gain 2 (V _{CM} = ±1.0 V, f ≤ 100 kHz)
Gain 2 (V _{CM} = ±1.0 V, f = 5.0 MHz)	—	60	—	—	—	
Supply Voltage Rejection	PSR	50	70	—	dB	
Output Offset Voltage	V _{OO}	—	0.6	2.0	V	
						Gain 1
Gain 2 and Gain 3	—	0.35	1.5	—	—	
Output Common Mode Voltage (Gain 3)	V _{CMO}	2.4	2.9	3.4	V	
Output Voltage Swing (Gain 2)	V _O	3.0	4.0	—	V _{p-p}	
Output Sink Current (Gain 2)	I _{Sink}	2.5	3.6	—	mA	
Output Resistance	R _{out}	—	20	—	Ω	
Power Supply Current (Gain 2)	I _D	—	18	24	mA	

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ELECTRICAL CHARACTERISTICS ($V_{CC} = +6.0$ Vdc, $V_{EE} = -6.0$ Vdc, @ $T_A = T_{high}$ to T_{low} , unless otherwise noted.)*

Characteristics	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain	AVD	250	—	600	V/V
Gain 1 (Note 2)					
Gain 2 (Note 3)					
Gain 3 (Note 4)					
Input Resistance	R _{in}	8.0	—	—	kΩ
Input Offset Current (Gain 3)	I _O	—	—	6.0	μA
Input Bias Current (Gain 3)	I _{IB}	—	—	40	μA
Input Voltage Range (Gain 2)	V _{in}	±1.0	—	—	V
Common Mode Rejection	CMR	50	—	—	dB
Gain 2 ($V_{CM} = \pm 1.0$ V, $f \leq 100$ kHz)					
Supply Voltage Rejection	PSR	50	—	—	dB
Gain 2 ($\Delta V_S = \pm 0.5$ V)					
Output Offset Voltage	V _{OO}	—	—	1.5	V
Gain 1					
Gain 2 and Gain 3					
Output Voltage Swing (Gain 2)	V _O	2.5	—	—	V _{p-p}
Output Sink Current (Gain 2)	I _O	2.5	—	—	mA
Power Supply Current (Gain 2)	I _D	—	—	27	mA

* $T_{low} = 0^\circ\text{C}$ for MC1733. $T_{high} = +70^\circ\text{C}$ for MC1733C.

- NOTES:**
1. Derate dual-in-line package at 9.0 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required a heatsink may be necessary to limit maximum junction temperature at 150°C.
 2. Gain Select pins G_{1A} and G_{1B} connected together.
 3. Gain Select pins G_{2A} and G_{2B} connected together.
 4. All Gain Select pins open.

Figure 4. Maximum Allowable Power Dissipation

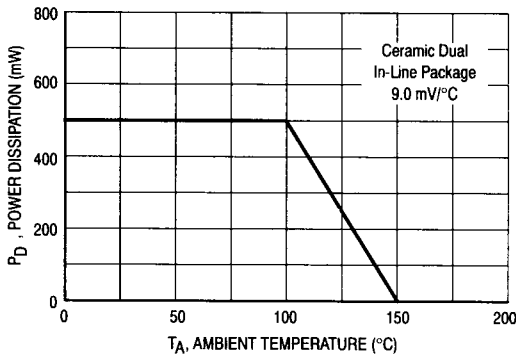


Figure 5. Supply Current versus Temperature

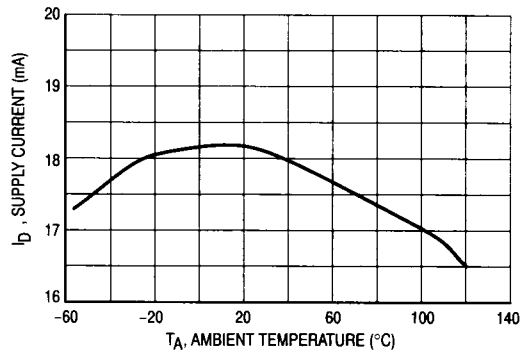


Figure 6. Supply Current versus Supply Voltage

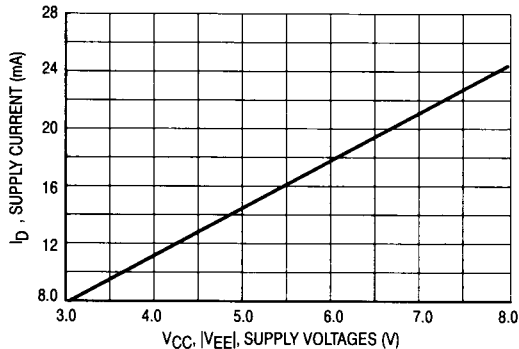


Figure 7. Gain versus Temperature

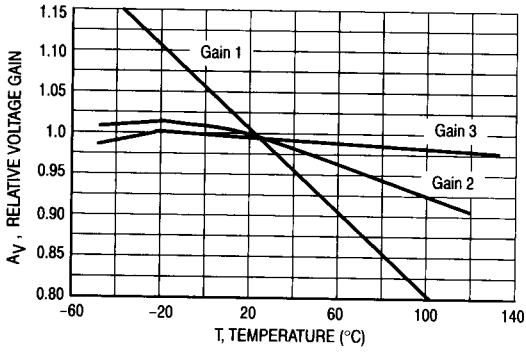


Figure 8. Gain versus Frequency

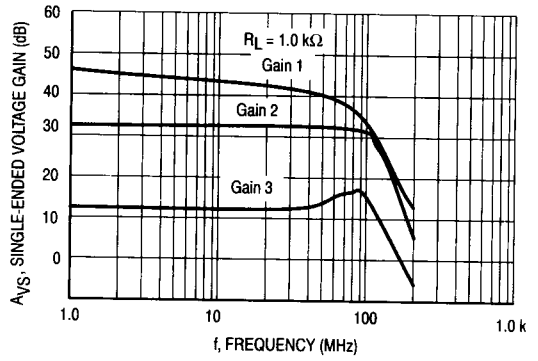


Figure 9. Gain versus Supply Voltage

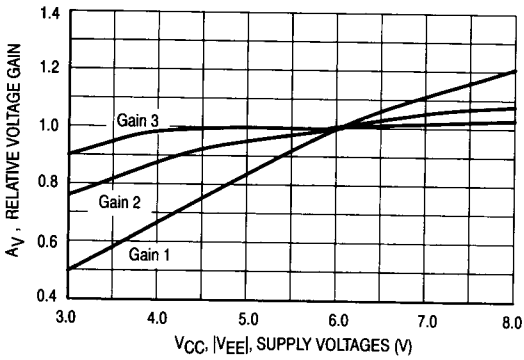


Figure 10. Gain versus R_{adj}

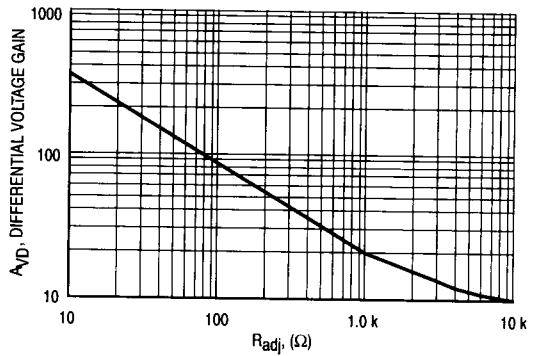


Figure 11. Gain versus Frequency and Supply Voltage

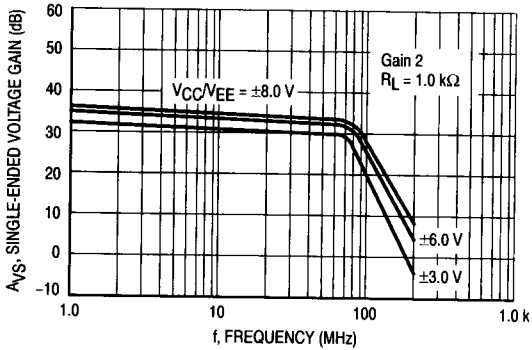


Figure 12. Gain versus Frequency and Temperature

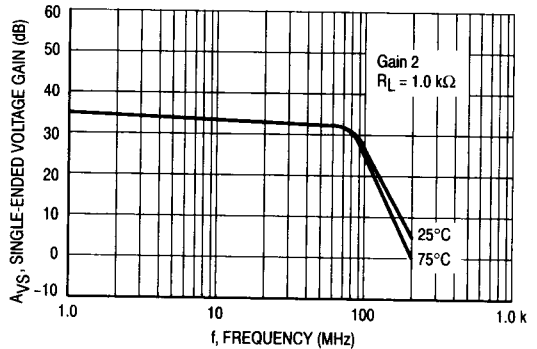


Figure 13. Pulse Response versus Gain

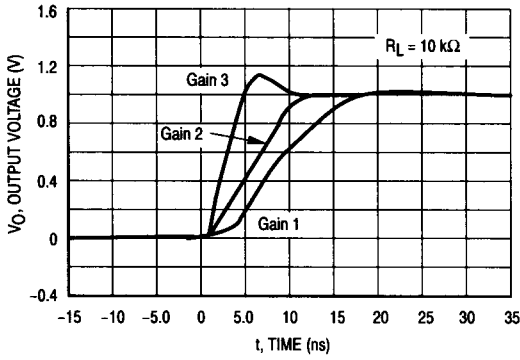


Figure 14. Pulse Response versus Supply Voltage

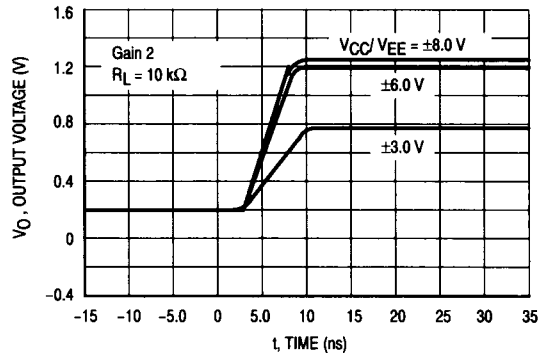


Figure 15. Pulse Response versus Temperature

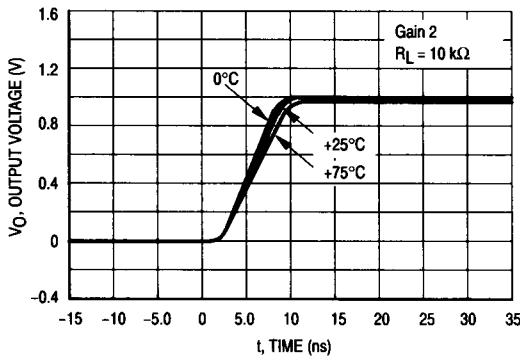


Figure 16. Differential Overdrive Recovery Time

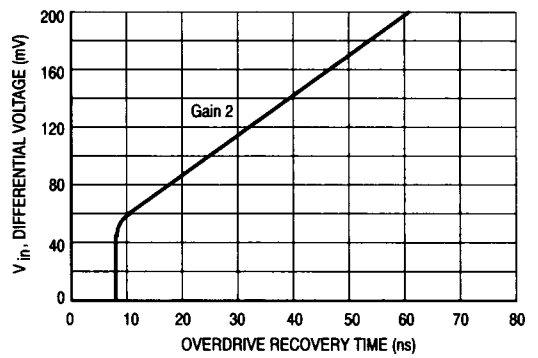


Figure 17. Phase Shift versus Frequency

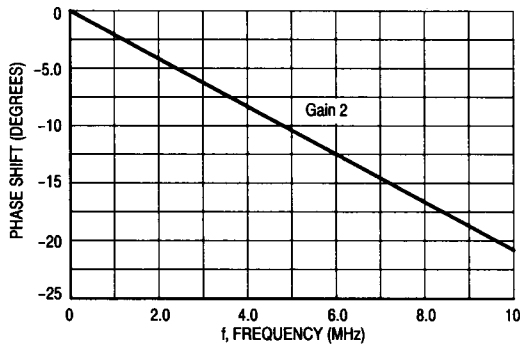
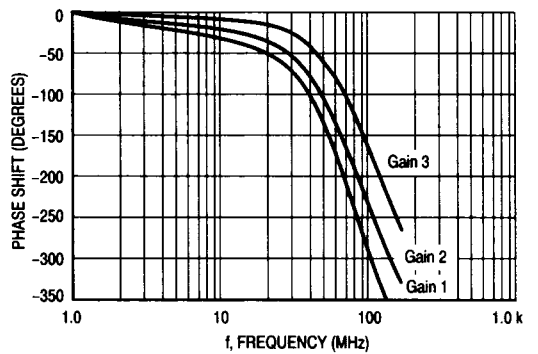


Figure 18. Phase Shift versus Frequency



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Figure 19. Input Resistance versus Temperature

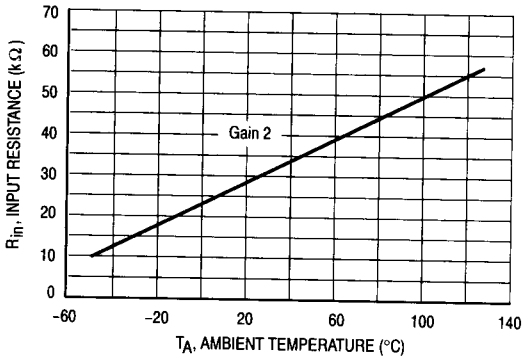


Figure 20. Input Noise Voltage

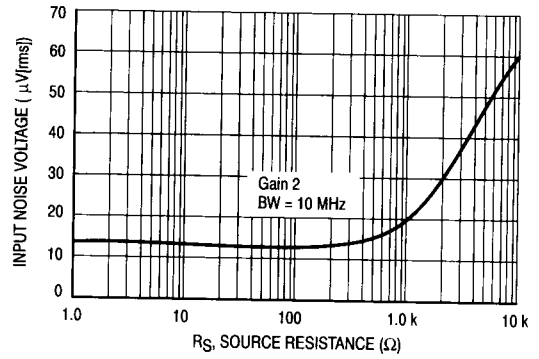


Figure 21. Output Voltage Swing and Sink Current versus Supply Voltage

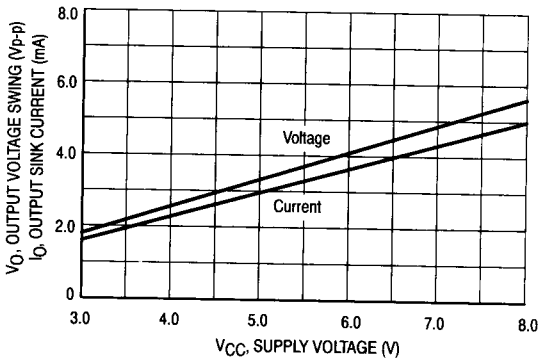


Figure 22. Output Voltage Swing versus Load Resistance

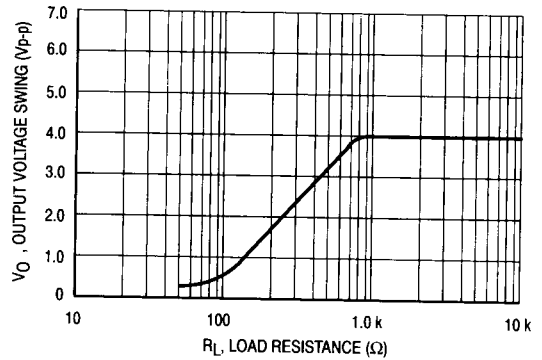


Figure 23. Output Voltage Swing versus Frequency

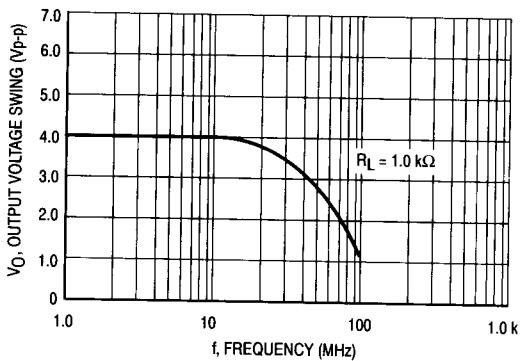


Figure 24. Common Mode Rejection Ratio

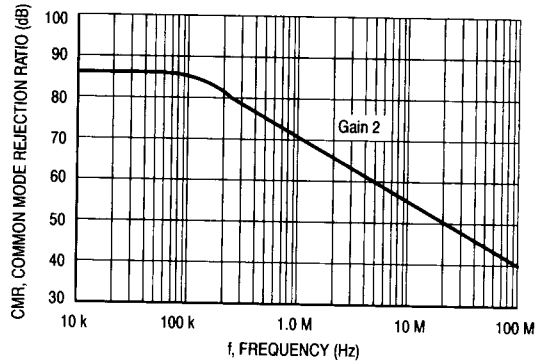
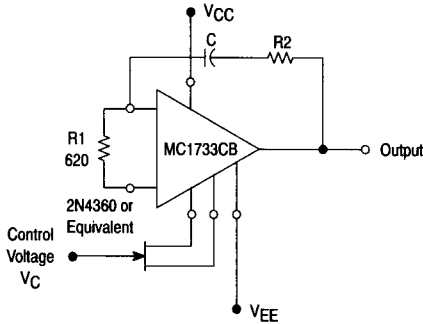
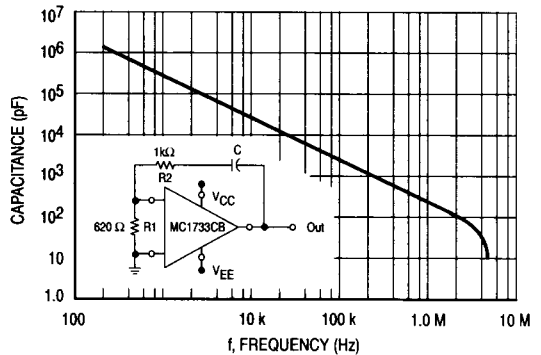


Figure 25. Voltage Controlled Oscillator



By changing the voltage V_C the gain will vary over a range of 10 V to 400 V. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

Figure 26. Oscillator Frequency for Various Capacitor Values



Tape, Drum or Disc Memory Read Amplifiers

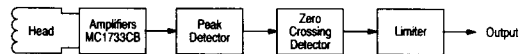
The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplification", increases the level of the signal available from the Read head to a level adequate to drive the Peak Detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7.0 mV to 25 mV for the signal from the Read head and 2.0 V for the signal to the Peak Detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 dB to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 dB to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, and MLM301. Equipment requiring higher transfer rates, such as disk systems normally use wideband amplifiers such as the MC1733CB. The actual crossover point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op amp, has approximately 20 dB open-loop gain at 100 kHz; the MC1733CB has approximately 33 dB of gain out to 100 MHz (depending on a gain option and loading).

There are a number of ways to implement the Peak Detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero crossing" for each of the data peaks in the Read signal.

Figure 27. Typical Read Circuit (Method 1)

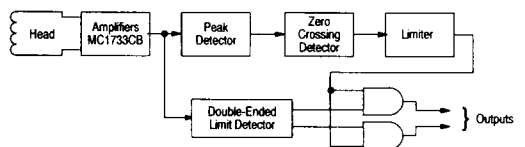


The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 30 dB. Thus, the 2.0 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the Zero Crossing Detector. In most cases detection of the zero crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100k B/S) comparators are used.

The method described above is often modified to include threshold sensing. In Figure 28, the function called Double Ended Limit Detector enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

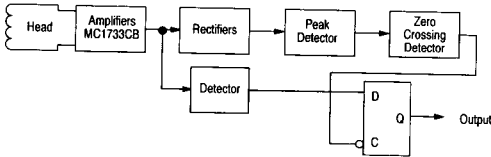
Figure 28. Read Circuit (Method 2)



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Another common technique is shown in Figure 29. The branch labeled rectifiers, Peak Detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the Peak Detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with preset threshold.

Figure 29. Read Circuit (Method 3)



The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then Method 1 may be the only feasible alternative.

Method 4 was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

Figure 30. Read Circuit (Method 4)

