15-2. The grounded-base h parameters for a 2N404 p-n-p germanium-alloy transistor are as follows ($I_E = 1$ ma, $V_C = -5$ volts, $T_A = 25°C$):

$$h_{ib} = 28 \text{ ohms} \qquad h_{rb} = 8 \times 10^{-4}$$
$$h_{fb} = 0.98 \qquad h_{ob} = 0.9 \ \mu\text{mho}$$

For the given bias and temperature conditions, calculate the low-frequency power gain for the grounded-emitter configuration, where $r_L = 20{,}000$ ohms and $r_g = 100$ ohms. Express the answer in decibels.

15-3. For the junction transistor described in Prob. 15-2, what should the values of r_L and r_g be for maximum grounded-emitter power gain? What is the matched power gain in decibels under these conditions?

15-4. Determine the maximum frequency of oscillation of an n-p-n germanium double-doped transistor (grown-junction process) at conditions of $I_E = -2$ ma, $V_C = 5$ volts, and $T_A = 25°C$. For this bar structure, the effective base width is 1 mil, the cross-sectional area is 100 mil^2, the base is uniform, having a resistivity of 0.2 ohm-cm, the collector is a step junction, and the collector resistivity is 4 ohm-cm. The contact to the base region is a single-line contact along one side of the bar. For this problem, assume that $\alpha \approx 1$ and that the only significant signal delay is due to base transit, such that $1/\omega_{\alpha b} \approx 1/\omega_b$.

15-5. Calculate G_e at 70 megacycles for the n-p-n silicon planar-epitaxial transistor described in Prob. 14-3 at the operating conditions of $V_{CE} = 20$ volts, $I_E = -10$ ma, and $T_A = 25°C$. Assume that at this level of current density, the active base resistance is between the edge of the diffused emitter and the inside edge of the base contact.

15-6. A p-n-p silicon microalloy transistor is to be designed for high power gain at a particular frequency. What base resistivity (uniform impurity profile) is required for maximum G_e? Assume that the majority-carrier mobility is the same as the corresponding minority value and that the alpha-cutoff frequency is determined only by the base-cutoff frequency ω_b.

15-7. A p-n-p germanium mesa transistor consists of a pair of 1×2 mil stripes (emitter and base) separated by 0.5 mil. f_T for this transistor is 500 megacycles and is assumed to be limited only by the $r_e C_{T_e}$ time constant. The effective C_c is 0.4 $\mu\mu f$. It is desired to scale up this structure for high-power operation. What is the maximum emitter edge length of the final design if the tuned output impedance of the final power transistor is not to be less than 10 ohms?

REFERENCES

1. Hunter, L. P.: Handbook of Semiconductor Electronics, chap. 11, p. 20, McGraw-Hill Book Company, Inc., New York, 1956.
2. Pritchard, R. L.: Unpublished memo reports, General Electric Research Laboratory, Schenectady, New York.
3. Pritchard, R. L.: High-frequency Power Gain of Junction Transistors, *Proc. IRE*, vol. 43, pp. 1075–1085, September, 1955.
4. Pritchard, R. L.: Frequency Response of Grounded-base and Grounded-emitter Transistors, AIEE Winter Meetings, New York, January, 1954.
5. Early, J. M.: Structure-determined Gain-band Product of Junction Triode Transistors, *Proc. IRE*, vol. 46, pp. 1924–1927, December, 1958.
6. Roach, William E.: Transistor Scaling Theory, Pacific Semiconductor, Inc., 1960.
7. Giacoletto, L. J.: Comparative High-frequency Operation of Junction Transistors Made of Different Semiconductor Materials, *RCA Rev.*, vol. 16, pp. 34–42, March, 1955.

16

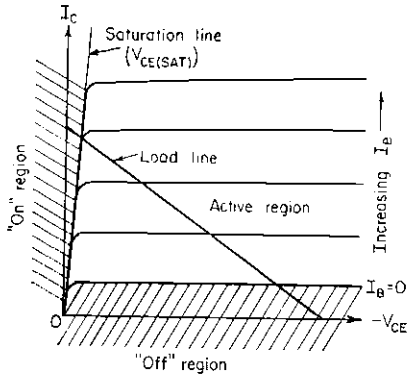
Junction-transistor Switches

16-1. Introduction to Switching Transistors. In addition to its use as an amplifier, the junction transistor serves as an excellent switching device for use in electronic computers or other forms of switching circuitry. Although switching circuits are many and varied, one can readily establish the fundamental requirements for the active element of the circuit for optimum switching performance. Let us examine these requirements in the light of an ideal switching transistor.

In general, a switching transistor has two states of conduction; it is either on or off. For the switch to be ideal, the off state must have a very high resistance, approaching that of an open circuit. In the on state, on the other hand, the ideal transistor switch should have a very low resistance, approaching that of a short circuit. In either case, the objective is to minimize the load power dissipated within the switch, whether it is on or off. The amount of power required to drive the ideal switch from one state to the other should be as small as possible.* Furthermore, the ideal device should be capable of switching large amounts of power; i.e., it should be able to withstand large voltages during the off condition and large currents during the on condition. Finally, in changing from one state to the other, the transistor should be able to switch as rapidly as possible. This requires that the transistor respond to the driving signal instantaneously. In other words, the transistor should have a very high gain-bandwidth response. It becomes apparent from the foregoing that the criteria for a junction-transistor switch have been established. In this chapter we shall discuss, in particular, the large-signal transient response of the transistor in order to relate the significant switching characteristics to the basic electrical parameters of the device.

* There is a lower practical limit to driving power, since it would not be desirable to have a device so sensitive that random noise pulses would cause it to switch.

In transistor switching circuits, the grounded-emitter configuration is by far the most widely used. For this arrangement, we shall be concerned with the collector output characteristic, since this will enable us to clearly understand the mechanism of switching from one state to another. A typical $V_C - I_C$ characteristic for a p-n-p junction transistor is given in Fig. 16-1. Examining this figure, we see that the output characteristic is divided into three defined regions of operation,[1,2,*] namely, the off region, the active region, and the on region. Each of these regions will be detailed separately.



Region	Emitter	Collector
Off	Reverse	Reverse
Active	Forward	Reverse
On	Forward	Forward

FIG. 16-1. Collector output characteristic for a p-n-p grounded-emitter transistor, illustrating three operating regions.

In the off region there exists the situation in which both the emitter and collector junctions are reverse-biased. Under these conditions, the collector current is very small, resulting in a large output impedance. As was shown in Chap. 9, the magnitude of this current is on the order of I_{CES}. It is seen that the off region is bounded by the curve for $I_B = 0$. This corresponds to the point of zero applied voltage to the base-to-emitter junction and also represents the boundary for the active region of the transistor. In Fig. 16-2 is a sketch of the minority-carrier concentration (holes) in the base layer for each of the three regions.[2] For the off condition, since both junctions are reverse-biased, the hole concentration is zero at the junctions, as shown. At the approximate center of the base layer, the hole concentration is equal to the equilibrium value.

* References, indicated in the text by superscript figures, are listed at the end of the chapter.

In the active region we have the normal mode of operation for the junction transistor; that is, the emitter is forward-biased and the collector is reverse-biased. In switching from off to on, the active region is traversed along the load line, as indicated in Fig. 16-1. As we shall see later, the speed of transition through the active region (transient response) is a function of the gain and frequency response in that region. The minority-carrier concentration for the active region, as shown in Fig. 16-2, is the familiar form discussed in previous chapters.

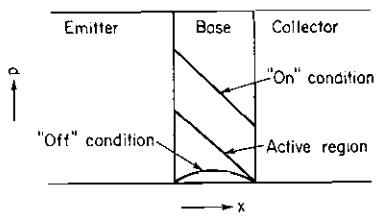


FIG. 16-2. Minority-carrier concentrations in the base layer as related to the region of operation.

The last of the three regions of operation is the on region, which is often referred to as a *saturation* condition. In this mode, the collector bias reverses polarity such that both emitter and collector junctions are forward-biased. As was shown in Sec. 9-8, the forward-bias potential of the emitter junction is slightly greater than that of the collector, resulting in a net negative potential from collector to emitter. This potential is represented by the saturation line drawn in Fig. 16-1, the slope of which corresponds to the saturation resistance of the transistor in the on condition. As is evident from Eq. (9-80), $V_{CE(SAT)}$ also includes the effect of any series resistance in the collector region. The hole concentration in the base layer for the on condition is also included in Fig. 16-2. At the collector junction, the hole concentration increases significantly because of the forward-bias condition at the collector. However, the slope of the hole concentration in the on condition remains the same as that at the edge of the active region, in order to maintain the same collector current.

The next section will present a physical description of the mechanisms that take place as the transistor is switched through the three defined regions of operation.

16-2. Qualitative Description of Switching Process. Before we establish a specific mathematical analysis of the switching transistor, it would be appropriate to present a qualitative description of the physical events that occur when a transistor is switched from off to on and then to off again. Let us refer to the basic switching circuit shown in Fig. 16-3, in which the transistor is driven by a constant base-current source. When the transistor is turned on, the collector current I_C flows for an input base current I_{B1}. The potential $V_{BE(OFF)}$ holds the transistor in the

off state because of the reverse-biased emitter. The generator in the base circuit is a pulse generator and is assumed to generate an ideal step-function input pulse. For this circuit, the waveforms that are observed for the base and collector current pulses, respectively, are as shown in Fig. 16-4. One observes that the output collector pulse is far from being an exact replica of the input base pulse. The reasons for these particular wave-shape discrepancies will be explained in the paragraphs to follow.

At time t_0, the pulse generator delivers a step base current to the transistor. At this instant, the transistor is sitting in the off condition because of the emitter reverse-bias voltage $V_{BE(\text{OFF})}$. The collector current that is flowing is extremely low (on the order of I_{CES}); since this is negligible, the voltage on the collector junction is equal to the sum of the supply voltage V_{CC} and the turnoff voltage $V_{BE(\text{OFF})}$. After t_0, the base current rises immediately to I_{B1}, but it is observed that the collector current does not begin to increase until t_1. The time between t_0 and t_1 is called the *delay time* t_d and is defined as the time required to bring the transistor from the initial off condition to the edge of conduction, i.e., to the beginning of the active region. This may be defined as that instant of time, t_1, at which the applied base-to-emitter voltage is zero. Physically, the finite time required for t_d comes about because of the reverse bias on both the emitter and collector junctions. As the effective base-to-emitter voltage goes from $V_{BE(\text{OFF})}$ to zero, the depletion layers on both junctions must reduce in thickness accordingly. This corresponds to an increase in the junction capacitances; the delay time is the time required to charge these capacitances to the new voltage level. It should be apparent that if $V_{BE(\text{OFF})} = 0$, then $t_d = 0$.

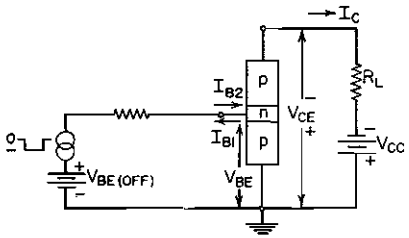


FIG. 16-3. Basic grounded-emitter transistor switching circuit. The base is driven by a constant-current source.

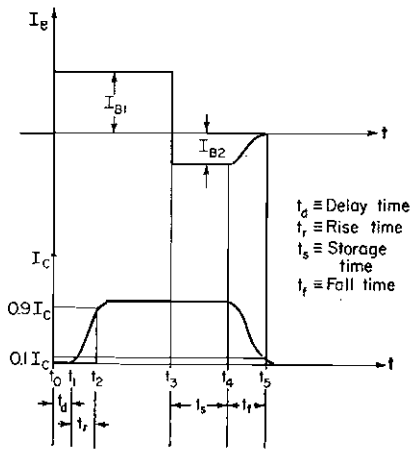


FIG. 16-4. Input base-current waveform and output collector-current waveform for a transistor, illustrating definition of switching times.

At time t_1, the operating point of the transistor is at the beginning of the active region, in which the emitter starts to become forward-biased and begins to inject current into the base. Now the collector current begins to increase toward its saturation value, corresponding approximately to V_{CC}/R_L. However, rather than increasing instantaneously at t_1, it requires a finite time to reach 90 per cent of the final value. This occurs at time t_2; the time interval $t_2 - t_1$ is defined as the *rise time* t_r of the collector current pulse. Rise time is attributed to the fact that there exists a finite transit delay between the base and collector currents and is a manifestation of the frequency response and current gain (beta) of the active region of the transistor. It should be recognized that neither the gain nor the frequency response remains constant through the active region. D-c beta (h_{FE}) will vary with current for the reasons already discussed in Chap. 10 and may pass through a maximum value depending on the $h_{FE}(I_C)$ characteristic and the magnitude of current to be switched. Also, the effective base width increases as the collector voltage decreases from the supply value to the saturation value. This, in turn, causes the base-transit time to increase so that the frequency response falls off.

During the same active switching interval, both the emitter and collector transition capacitances must be charged to account for the depletion-layer changes with voltage. In the emitter, the capacitance increases because the contact potential is reduced by the forward-bias portion of V_{BE}; in the collector, the capacitance also increases and must be charged through the collector series resistance, which is predominantly the external load resistor R_L. All these effects take place simultaneously and will be analyzed quantitatively to determine the collective effect on rise time.

The transistor will remain in the on state as long as the input base current I_{B1} is maintained. With reference to Fig. 16-4 again, at time t_3 the base input pulse steps off immediately; however, it is observed that the collector pulse does not respond until time t_4. The time interval between t_3 and t_4 is referred to as the *storage time* t_s and is attributed to the same basic storage phenomenon described in Chap. 6 for the p-n junction. The storage time is a measure of the time required for the minority carriers in the base and collector to recombine back to the level corresponding to the boundary between the active and saturation regions. These excess carriers arise because the collector junction becomes forward-biased when the base current I_{B1} is greater than the I_B necessary to produce I_C; i.e., $I_{B1} > I_C/h_{FE}$. Thus, storage time is related to a carrier-recombination process and is a measure of the minority-carrier lifetime in the base and collector regions.

Finally, at time t_4, the transistor comes out of saturation and the

operating point traverses the load line again through the active region into the off state. This is the turnoff portion of the collector waveform; the time interval between t_4 and t_5 is defined as the *fall time* t_f. At t_5, the collector current has reduced to $0.1I_C$. The description of the switching process for fall time is similar to that for rise time, except that the active region is traversed in the reverse direction.

In summary, we see that in response to a step input of base current, the collector current requires a total *turnon time*, which is

$$t_{ON} = t_d + t_r \tag{16-1}$$

Also, when the base current is removed as a step, the collector current requires a total *turnoff time*, which is

$$t_{OFF} = t_s + t_f \tag{16-2}$$

16-3. Stored-base-charge Transistor Analysis. In all the analyses of the transistor that have appeared in the preceding chapters, the theory has been based on the argument that the transistor is a current-controlled device; i.e., the collector current is affected by changes in either the emitter current or base current. Thus, the basic equations derived for d-c characteristics, h parameters, frequency response, etc., are all a function of the currents of the transistor. Without a doubt, this is a very appropriate and worthwhile approach to analyzing the transistor theoretically from either the steady-state or small-signal point of view, because one can readily approximate linear operation for the transistor. However, when one has to apply a large-signal analysis to the transistor, as is the case in describing switching characteristics, the current approach becomes relatively complex because of the high degree of nonlinearity displayed by the transistor for large changes in current and/or voltage.

To aid in the large-signal analysis of the switching transistor, a powerful new concept has been introduced by Beaufoy and Sparkes, in which they regard the transistor as a *charge-controlled* device.[3] In this concept, the collector current is related to the charge in the base; in order to effect a change in collector current there must be a change in the total charge in the base. For example, in the grounded-emitter transistor, the base current provides the necessary total base charge which controls the collector current.

The fundamental relationship in charge-control transistor theory is the obvious fact that current is charge per unit time, or

$$\Delta I = \frac{\Delta Q}{\tau} \tag{16-3}$$

where τ is defined as a time constant which relates the current to the charge. Therefore, if we are to relate the collector current I_C to the total

base charge Q_B, the collector time constant τ_C is Q_B/I_C. In a similar manner, the emitter and base currents can be related to Q_B, so that we have

Emitter time constant: $$\tau_E = \frac{Q_B}{I_E} \tag{16-4}$$

Base time constant: $$\tau_B = \frac{Q_B}{I_B} \tag{16-5}$$

Collector time constant: $$\tau_C = \frac{Q_B}{I_C} \tag{16-6}$$

We shall now proceed to relate these time constants to the characteristics of the transistor. Let us consider the active region of the p-n-p transistor in which the emitter is forward-biased and the collector is reverse-biased. Under these conditions, the emitter is injecting holes into the base, and if $W \ll L_{pb}$, then a linear hole gradient is established in the base which decreases to zero at the collector. As was shown in Chap. 8, the emitter current is given by

$$I_E = -qAD_{pb}\frac{dp}{dx} \tag{16-7}$$

In the base region,

$$\frac{dp}{dx} \approx -\frac{p_{nb}\epsilon^{qV_E/kT}}{W} \tag{16-8}$$

so that Eq. (16-7) becomes

$$I_E \approx \frac{qAD_{pb}p_{nb}\epsilon^{qV_E/kT}}{W} \tag{16-9}$$

But $qAp_{nb}\epsilon^{qV_E/kT}$ is the charge per unit length just at the base side of the emitter junction ($x = 0$); it decreases linearly to zero at $x = W$. Therefore, the total charge in the base is the area of the charge gradient (triangle), or

$$Q_B = \frac{qAp_{nb}\epsilon^{qV_E/kT}W}{2} \tag{16-10}$$

Substituting Eq. (16-10) into (16-9), we obtain

$$I_E \approx \frac{2D_{pb}Q_B}{W^2} \tag{16-11}$$

From Eq. (9-13) for $\gamma \approx 1$ we see that $W^2/2D_{pb}\tau_{eff} \approx I_B/I_E$, so that Eq. (16-11) becomes, finally,

$$I_B = \frac{Q_B}{\tau_{eff}} \tag{16-12}$$

Thus we see that the base time constant τ_B is equal to the effective minority-carrier lifetime in the base; i.e., surface recombination is

included. In other words, base current flows to maintain the total base charge constant by making up for the amount of charge being lost by recombination.

To determine the emitter time constant, we refer to Eq. (16-11), where we saw that

$$\tau_E = \frac{Q_B}{I_E} = \frac{W^2}{2D_{pb}} = \tau_B(1 - \alpha) \tag{16-13}$$

From Eq. (14-8), we see that for the uniform base, the base-cutoff frequency is given as

$$\frac{1}{\omega_b} = \frac{W^2}{2.43D_{pb}} \tag{16-14}$$

Substituting this result into Eq. (16-13), we have[3]

$$\tau_E = \frac{1.2}{\omega_b} \qquad \text{uniform base} \tag{16-15}$$

For a graded base, it was shown in Sec. 8-7 that $\tau_E \approx W^2/4D_{pb}$; therefore,

$$\tau_E = \frac{0.6}{\omega_b} \qquad \text{graded base} \tag{16-16}$$

where ω_b is already corrected by the ln (N'_B/N_{BC}) term.

Finally, for the collector time constant, since $I_C = \alpha I_E$, we get, simply,

$$\tau_C = \frac{\tau_E}{\alpha} \tag{16-17}$$

With each of the time constants defined, we are now in a position to apply them to the large-signal transient response of the transistor. The basic equation is the equation of charge continuity, which is [3,4]

$$I = \frac{dQ}{dt} + \frac{Q}{\tau} \tag{16-18}$$

If this result is integrated over a given time interval, then

$$\int_0^t I\,dt = \int_{Q_1}^{Q_2} dQ + \int_0^t \frac{Q\,dt}{\tau} \tag{16-19}$$

This says that the total charge supplied during the interval t is equal to the amount of charge necessary to change the current in the volume to a new level plus the amount necessary to replenish that lost by recombination. Herein lies the beauty of the charge concept for large-signal analysis. In solving Eq. (16-19), one is concerned only with the absolute total change of charge during the time interval as determined by the limits of integration, thereby eliminating any concern for the variations of the time constants during the same interval.

In order to attach physical meaning to all of the foregoing, we shall now present a qualitative description[3] of how the total base charge of a grounded-emitter transistor changes as the base current shifts suddenly from I_{B1} to a new level I_{B2}. In this particular situation, we shall assume that the switching all takes place in the active region. Reference is made to the switching circuit of Fig. 16-3 and the base-charge diagram in Fig. 16-5. At the initial current level, the charge distribution in the base appears as the unshaded portion of Fig. 16-5. The charge level below

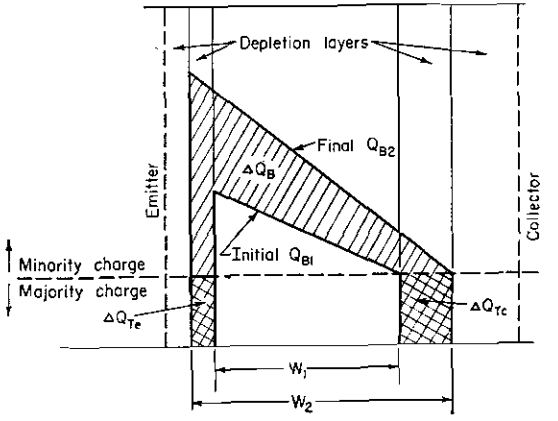


FIG. 16-5. Base-charge distributions illustrating switching in the active region. The shaded area denotes additional stored charge.

the dashed line corresponds to the equilibrium majority-carrier electrons in the n-type base. The charge above the dashed line represents the minority-carrier hole concentration injected by the emitter. This hole gradient is matched by an equal charge of electrons injected by the base in order to maintain neutrality.[3] Also shown in Fig. 16-5 are the depletion layers of the emitter and collector junctions, which have spread to establish the effective base width W_1. Thus, we have described the nature of the base charge at the initial active condition where the base current I_{B1} produces a collector current I_{C1}.

When I_{B1} is switched rapidly to I_{B2}, several changes occur simultaneously. Firstly, the increased forward-bias potential at the emitter causes the depletion layer to narrow, corresponding to an increase in the emitter transition capacitance. Secondly, the level of injected holes increases and the gradient steepens, corresponding to the new level of collector current I_{C2}. Thirdly, the increase in collector current causes the collector junction voltage to decrease due to the larger voltage drop across the load resistor R_L. This causes the collector depletion layer to narrow, establishing an increase in the collector transition capacitance.

Finally, because of both depletion-layer variations, the base width increases from its initial value W_1 to its final value W_2.

To account for all the changes described, an additional charge, equal to all the shaded area shown in Fig. 16-5, must be injected into the base region. This charge is composed of several parts. Below the dashed line, the shaded regions represent the amount of majority-electron charges necessary to neutralize the impurity ions exposed by the reduced depletion regions. These are denoted by ΔQ_{Te} and ΔQ_{Tc}, the additional charges in the transition capacitances of the junctions. The shaded area above the dashed line is the charge required to set up the new current level and maintain it against the recombination rate. This area also includes the extra base charge required to compensate for the increased base width or, more specifically, to charge up the emitter and collector diffusion capacitances. It should be recalled that diffusion capacitance is the amount of charge that must be added or removed from the base when a voltage variation causes the base width to change; i.e., $C_D = dQ/dV$. To express the total base-charge variation mathematically, we use the form of Eq. (16-19).[3,5,6]

$$\int_0^t I_B\,dt = \int_{Q_{Te1}}^{Q_{Te2}} dQ_{Te} + \int_{Q_{Tc1}}^{Q_{Tc2}} dQ_{Tc} + \int_{Q_{B1}}^{Q_{B2}} dQ_B + \int_0^t \frac{Q_B\,dt}{\tau_B} \tag{16-20}$$

Since the first two right-hand terms represent the transition-region charges, we can change their limits of integration, and we have

$$\int_0^t I_B\,dt = \int_{V_{BE1}}^{V_{BE2}} C_{Te}\,dV_{BE} + \int_{V_{CB1}}^{V_{CB2}} C_{Tc}\,dV_{CB} + \int_{Q_{B1}}^{Q_{B2}} dQ_B + \int_0^t \frac{Q_B\,dt}{\tau_B} \tag{16-21}$$

It was the purpose of this section to illustrate the general application of the base-charge theory to the solution of large-signal transistor problems. In the sections to follow, the concept will be utilized to derive the specific equations for the delay, rise, storage, and fall times of the transistor in the switching circuit of Fig. 16-3.

16-4. Delay Time. In Sec. 16-2, delay time t_d was defined as the time required to bring the transistor from the initial off condition to the edge of the active region. To do this, the base requires a total charge equal to that necessary to charge the transition capacitances of the emitter and collector junctions as the voltage changes by the amount $\Delta V = V_{BE(\text{OFF})}$. Since we are at the edge of conduction, we can assume that $I_C = 0$ (neglecting I_{CES}), and therefore $Q_B \approx 0$. The charge equation is written as[7]

$$I_B = \frac{dQ_{Te}}{dt} + \frac{dQ_{Tc}}{dt} \tag{16-22}$$

Integrating this result with respect to time and changing the limits, we have

$$\int_0^{t_d} I_B\,dt = \int_{-V_{BE(\text{OFF})}}^{0} C_{Te}\,dV_{BE} + \int_{-(V_{CC}+V_{BE(\text{OFF})})}^{-V_{CC}} C_{Tc}\,dV_{CB} \tag{16-23}$$

where V_{CC} is the collector supply voltage. In this equation we cannot assume that the transition capacitances are constants, since we know that they vary as $V^{-1/n}$. In most transistors, the emitter approximates a step junction, and therefore C_{Te} varies as $V_{BE}^{-1/2}$, or

$$C_{Te} = C'_{Te}V_{BE}^{-1/2} \tag{16-24}$$

where C'_{Te} is the emitter capacitance measured at a total voltage $(V_{BE} + V_T)$ equal to 1 volt. Further, for the collector capacitance it may be assumed that C_{Tc} varies as $V_{CB}^{-1/2}$, regardless of whether the junction is a step or is graded. This is so for the graded case as long as the magnitude of V_{CC} is high enough to establish square-root behavior. At lower values of V_{CC}, C_{Tc} will vary as $V_{CB}^{-1/2.5}$ or $V_{CB}^{-1/3}$. Nevertheless,

$$C_{Tc} \approx C'_{Tc}V_{CB}^{-1/2} \tag{16-25}$$

where C'_{Tc} is the collector capacitance for $(V_{CB} + V_T) = 1$ volt. Substituting Eqs. (16-24) and (16-25) into Eq. (16-23) and integrating, we have

$$I_{B1}t_d = 2C'_{Te}V_{BE(\text{OFF})}^{1/2} + 2C'_{Tc}[(V_{CC} + V_{BE(\text{OFF})})^{1/2} - V_{CC}^{1/2}] \tag{16-26}$$

or, finally,

$$t_d = \frac{2}{I_{B1}}\{C'_{Te}V_{BE(\text{OFF})}^{1/2} + C'_{Tc}[(V_{CC} + V_{BE(\text{OFF})})^{1/2} - V_{CC}^{1/2}]\} \tag{16-27}$$

Thus we see that the delay time increases with the magnitude of the turnoff voltage $V_{BE(\text{OFF})}$ and decreases as the turnon base current I_{B1} becomes larger. From a transistor-design point of view, since the second term of Eq. (16-27) is usually negligible when $V_{BE(\text{OFF})} \ll V_{CC}$, we see that delay time is minimized when the emitter transition capacitance is small. This means that one should design for small emitter areas primarily.

16-5. Rise Time. Rise time t_r is defined as the time required for the collector current to increase to 90 per cent of its final value in the switching circuit. Essentially, this transition occurs completely in the active region of the transistor, starting at the edge of conduction and ending just below the edge of saturation. Based on the discussions in the earlier sections, we can write the charge equation as[3,6]

$$I_B = \frac{dQ_{Te}}{dt} + \frac{dQ_{Tc}}{dt} + \frac{dQ_B}{dt} + \frac{Q_B}{\tau_B} \tag{16-28}$$

where τ_B is the base time constant. The first right-hand term corresponds to the charging of the emitter junction capacitance as the forward-bias voltage reduces the junction contact potential; the second term corresponds to the charging of the collector capacitance as the collector voltage decreases with increasing current; the third and fourth terms represent the charging of the base region to attain the new collector-current level and maintain it against the recombination rate.

Eq. (16-28) is a first-order differential equation and may be readily solved by separation of variables. It may be arranged as

$$\frac{1}{I_B - Q_B/\tau_B} = \frac{dt}{dQ_{Te} + dQ_{Tc} + dQ_B} \tag{16-29}$$

Since we are interested in a solution in terms of collector current I_C, we can multiply both sides of Eq. (16-29) by dI_C and integrate the result. Since the collector current increases from 0 to $0.9I_C$ during the time interval from 0 to t_r, we have, finally,

$$\int_0^{0.9I_C} \frac{dI_C}{I_{B1} - Q_B/\tau_B} = \int_0^{t_r} \frac{dt}{dQ_{Te}/dI_C + dQ_{Tc}/dI_C + dQ_B/dI_C} \tag{16-30}$$

Note that $I_B = I_{B1}$, since we are assuming that the base current steps up instantaneously at the start of turnon. The dQ/dI_C terms in the denominator of Eq. (16-30) are time constants as defined by Eq. (16-3). The emitter time constant is given by

$$\frac{dQ_{Te}}{dI_C} = \frac{1}{I_C}\int_{Q_{Te1}}^{Q_{Te2}} dQ_{Te} = \frac{1}{I_C}\int_{V_{BE1}}^{V_{BE2}} C_{Te}\, dV_{BE} \tag{16-31}$$

During the rise-time interval, the applied emitter voltage changes from 0 to approximately $V_T/2$, where V_T is the junction contact potential. Assuming a step junction,

$$\frac{dQ_{Te}}{dI_C} \approx \frac{1}{I_C}\int_0^{V_T/2} \frac{C'_{Te}\, dV_{BE}}{V_{BE}^{1/2}} = \frac{2C'_{Te}(V_T/2)^{1/2}}{I_C} \tag{16-32}$$

where C'_{Te} is the capacitance at 1 volt. However, Eq. (16-32) can be modified such that

$$\frac{dQ_{Te}}{dI_C} \approx \frac{C_{Te}V_T}{I_C} \tag{16-33}$$

where C_{Te} is the emitter capacitance at the final current level. Since V_T/I_C is the d-c junction resistance, we can approximate the time constant as

$$\frac{dQ_{Te}}{dI_C} \approx R_E C_{Te} \approx \frac{1}{\omega_e} \tag{16-34}$$

In a similar manner, the collector-junction time constant is given by

$$\frac{dQ_{Tc}}{dI_C} = \frac{1}{I_C}\int_{Q_{Tc1}}^{Q_{Tc2}} dQ_{Tc} = \frac{1}{I_C}\int_{V_{CB1}}^{V_{CB2}} C_{Tc}\, dV_{CB} \tag{16-35}$$

Assuming that the collector depletion layer varies as $V_{CB}^{1/2}$, we have

$$\frac{dQ_{Tc}}{dI_C} \approx \frac{1}{I_C}\int_{-V_{CC}}^{-V_{CE(SAT)}} \frac{C'_{Tc}\, dV_{CB}}{V_{CB}^{1/2}} \approx \frac{2C'_{Tc}V_{CC}^{1/2}}{I_C} \tag{16-36}$$

In this result, the $V_{CE(SAT)}$ term is neglected because it is usually quite small compared to V_{CC}. We can express Eq. (16-36) in terms of capacitance at the initial voltage V_{CC}. Also, we recognize that[7,8]

$$R_L = \frac{V_{CC} - V_{CE(SAT)}}{I_C} \approx \frac{V_{CC}}{I_C} \tag{16-37}$$

Therefore, Eq. (16-36) becomes

$$\frac{dQ_{Tc}}{dI_C} \approx 2R_L C_{Tc} \qquad \text{step junction} \tag{16-38}$$

For a graded junction, where $C_{Tc} \propto V_{CB}^{-1/3}$, it is easily shown that

$$\frac{dQ_{Tc}}{dI_C} \approx 1.5R_L C_{Tc} \qquad \text{graded junction} \tag{16-39}$$

Thus we see that the charging of the collector capacitance through the load resistor can be a significant factor.[8] It should be understood that the collector resistance r_{SC} is in series with R_L but is neglected because we assume $V_{CE(SAT)}$ is small.

The final time constant in Eq. (16-30) is the dQ_B/dI_C term.

$$\frac{dQ_B}{dI_C} = \frac{1}{I_C}\int_{Q_{B1}}^{Q_{B2}} dQ_B = \frac{Q_{B2} - Q_{B1}}{I_C} \tag{16-40}$$

Since the initial total charge Q_{B1} is zero ($I_C \approx 0$),

$$\frac{dQ_B}{dI_C} \approx \frac{Q_{B2}}{I_C} = \tau_C \tag{16-41}$$

From Eqs. (16-15) to (16-17), we have

$$\frac{dQ_B}{dI_C} \approx \frac{1.2}{\alpha\omega_b} \qquad \text{uniform base} \tag{16-42}$$

$$\frac{dQ_B}{dI_C} \approx \frac{0.6}{\alpha\omega_b} \qquad \text{graded base} \tag{16-43}$$

where ω_b is the base-cutoff frequency at the edge of saturation.

Examining Eqs. (16-34), (16-38), (16-42), and (16-43), we see that they are in the form of

$$\frac{dQ_{Te}}{dI_C} + \frac{dQ_{Tc}}{dI_C} + \frac{dQ_B}{dI_C} \approx \frac{1}{\omega_e} + \frac{K}{\alpha\omega_b} + 2R_LC_{Tc} \tag{16-44}$$

However, the first two terms may be approximated by $1/\omega_T$, the current-gain bandwidth frequency (see Eq. 14-28), wherein we neglect the depletion-layer transit time since this is small at the edge of saturation. Therefore we obtain, finally,

$$\frac{dQ_{Te}}{dI_C} + \frac{dQ_{Tc}}{dI_C} + \frac{dQ_B}{dI_C} \approx \frac{1}{\omega_T} + 1.7R_LC_{Tc} \tag{16-45}$$

The constant multiplying R_LC_{Tc} has been selected as a nominal value to generalize the result for all transistor types. Thus Eq. (16-45) may be substituted into Eq. (16-30) to solve for t_r.

To integrate the left-hand part of Eq. (16-30), we recognize from Eqs. (16-13) and (16-17) that

$$\frac{Q_B}{\tau_B} = \frac{\tau_C I_C}{\tau_B} = \frac{I_C(1-\alpha)}{\alpha} = \frac{I_C}{h_{FE}} \tag{16-46}$$

Substituting this result into Eq. (16-30) and completing the integration, we have

$$t_r \approx h_{FE}\left(\frac{1}{\omega_T} + 1.7R_LC_{Tc}\right)\ln\frac{h_{FE}I_{B1}}{h_{FE}I_{B1} - 0.9I_C} \tag{16-47}$$

which is the final expression for rise time.* All terms except C_{Tc} are measured at the edge of saturation. One observes that the logarithm function is multiplied by both h_{FE} and a time constant which is the effective cutoff frequency of the transistor having R_L as a load resistor. The logarithm function times h_{FE} is called the *circuit-drive function* and is plotted in Fig. 16-6 as a function of alpha [$\alpha = h_{FE}/(1 + h_{FE})$] for different values of the circuit current ratio I_C/I_{B1}. It is apparent that this function (or rise time) is reduced by the choice of a high-h_{FE} transistor and high circuit drive (low I_C/I_{B1} ratio).

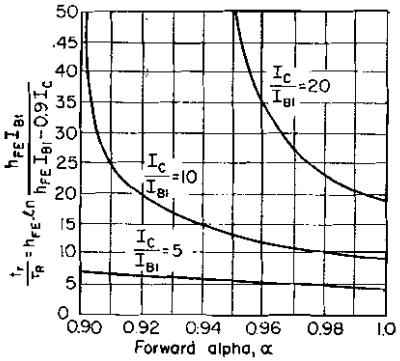


FIG. 16-6. Magnitude of circuit-drive function for rise time t_r.

From a transistor-design point of view, Eq. (16-47) indicates that low rise time is achieved with high f_T. Thus, the requirement for very small emitter and collector junction areas becomes extremely important if very high switching speeds are needed.

* This result is very similar to that given by Moll.[2]

16-6. Storage Time. Once the transistor is fully turned on, it remains in saturation because the driving base current I_{B1} is greater than that necessary to establish the collector current I_C, that is, $I_{B1} > I_C/h_{FE}$. In saturation, the collector junction becomes forward-biased and the charge diagram[3] appears as shown in Fig. 16-7. In the base region, the total stored charge in saturation is denoted by Q_{BS}. It is also seen that the carrier concentration at the collector is not zero, but has a finite value depending on the magnitude of the collector forward bias in saturation. Because the collector is injecting holes into the base (for p-n-p), one also has to consider the injection of electrons into the collector from the same junction potential. If the minority-carrier concentration in the collector is at all appreciable (high collector resistivity), the charge stored in the collector cannot be neglected. In Fig. 16-7, the collector charge is denoted by Q_{CS}. Thus the total stored transistor charge is $Q_{BS} + Q_{CS}$. If Q_B is the amount of base charge required to bring the transistor to the boundary between active and saturated operations, then the excess stored charge is

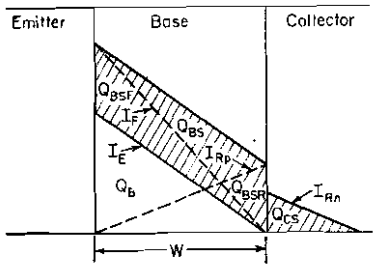


FIG. 16-7. Transistor charge distribution in saturation region. The shaded area denotes excess stored charge. Illustrated also is the stored charge in the collector region.

$$Q_X = Q_{BS} + Q_{CS} - Q_B \tag{16-48}$$

The crosshatched portions of Fig. 16-7 represent the excess charge Q_X.

Thus, storage time t_s is the time required for the transistor to come out of saturation, or specifically, the time required to reduce the excess charge to zero. The latter occurs when the collector forward potential is reduced to zero and starts to reverse polarity. The storage interval begins when the base current I_{B1} is reversed to a turnoff value I_{B2}. Since the excess base current may be defined as[3,9]

$$I_{BX} = I_{B1} - I_B \tag{16-49}$$

the storage time constant is

$$\tau_S = \frac{dQ_X}{dI_B} = \frac{Q_X}{I_{BX}} \tag{16-50}$$

To aid in the analysis of the saturation region, we can make use of the concept that the total base charge is made up of two components,[2]

$$Q_{BS} = Q_{BSF} + Q_{BSR} \tag{16-51}$$

where these total charges are defined by the regions shown in Fig. 16-7. The first term corresponds to a forward emitter-to-collector current I_F; the second term is a reverse collector-to-emitter current I_R. The latter current is

$$I_R = I_{Rp} + I_{Rn} \tag{16-52}$$

where I_{Rp} is the hole current injected into the base and I_{Rn} is the electron current injected into the collector. Substituting Eq. (16-51) into Eq. (16-48) and the latter into Eq. (16-50), we have

$$\tau_S = \frac{dQ_X}{dI_B} = \frac{Q_{BSF} + Q_{BSR} + Q_{CS} - Q_B}{I_{BX}} \tag{16-53}$$

or, in terms of time constants,

$$\tau_S = \frac{dQ_X}{dI_B} = \frac{\tau_E I_F + \tau_{ER} I_{Rp} + \tau_{CS} I_{Rn} - \tau_E I_E}{I_{BX}} \tag{16-54}$$

where τ_{ER} is the emitter time constant in the reverse direction and τ_{CS} is the time constant of the collector region. We can now proceed to simplify Eq. (16-54).

Firstly, if base recombination is sufficiently low so that base transport is unity in either direction, we can establish a reverse alpha given by the reverse collector efficiency as

$$\alpha_R = \gamma_R = \frac{I_{Rp}}{I_{Rp} + I_{Rn}} = \frac{I_{Rp}}{I_R} \tag{16-55}$$

From this relation, we see that $I_{Rp} = \alpha_R I_R$ and $I_{Rn} = (1 - \alpha_R) I_R$.

Secondly, to determine the expression for I_{BX} in terms of α_R and I_R, we refer to Eq. (16-49), in which[3]

$$I_{B1} = (1 - \alpha) I_F + (1 - \alpha_R) I_R \tag{16-56}$$

and

$$I_B = (1 - \alpha) I_E \tag{16-57}$$

Therefore

$$I_{BX} = (1 - \alpha)(I_F - I_E) + (1 - \alpha_R) I_R \tag{16-58}$$

Since $I_C = \alpha I_E = \alpha I_F - I_R$,

$$I_F - I_E = \frac{I_R}{\alpha} \tag{16-59}$$

Substituting Eq. (16-59) into Eq. (16-58) and simplifying, we obtain[3]

$$I_{BX} = \frac{I_R}{\alpha} (1 - \alpha\alpha_R) \tag{16-60}$$

Inserting Eq. (16-60) and the relations from Eq. (16-55) into Eq. (16-54) and rearranging, we obtain the final expression for the storage time constant,

$$\tau_S = \frac{dQ_X}{dI_B} = \frac{Q_X}{I_{BX}} = \frac{\tau_E + \alpha\alpha_R \tau_{ER}}{1 - \alpha\alpha_R} + \frac{\alpha(1 - \alpha_R)\tau_{CS}}{1 - \alpha\alpha_R} \tag{16-61}$$

This result will be discussed in the latter part of this section.

The equation for storage time t_s is obtained by solving the differential charge equation, which is[3]

$$I_B = \frac{Q_B}{\tau_B} + \frac{Q_{BS}}{\tau_S} + \frac{dQ_B}{dt} + \frac{dQ_{BS}}{dt} \tag{16-62}$$

Since the storage-time interval ends when $Q_{BS} = 0$, during that interval $dQ_B/dt = 0$; Q_B is constant during that time and equal to $\tau_C I_C$. Furthermore, during the same interval, I_B was switched to I_{B2}. Thus, Eq. (16-62) becomes

$$I_{B2} - \frac{\tau_C I_C}{\tau_B} - \frac{Q_{BS}}{\tau_S} = \frac{dQ_{BS}}{dt} \tag{11-63}$$

Introducing dI_B and separating the variables for integration, we obtain

$$\int_{I_{BX}}^{0} \frac{dI_B}{I_{B2} - \tau_C I_C/\tau_B - Q_{BS}/\tau_S} = \int_0^{t_s} \frac{dt}{dQ_{BS}/dI_B} \tag{16-64}$$

where $I_{BX} = I_{B1} - I_B$. Recognizing that τ_C/τ_B is $1/h_{FE}$ and that dQ_{BS}/dI_B is equal to τ_S, we obtain, as a complete solution for the storage time,

$$t_s = \tau_S \ln \frac{I_{B1} - I_{B2}}{I_C/h_{FE} - I_{B2}} \tag{16-65}$$

In this result, I_{B2} is negative, so that $|I_{B1} - I_{B2}|$ equals $|I_{B1}| + |I_{B2}|$. This is also true for the denominator.

The significant parameter in the storage-time equation is τ_S, as given by Eq. (16-61). For an alloy-type transistor having negligible collector stored charge, we can let $\alpha\alpha_R = 1$ and $\tau_{CS} = 0$, and Eq. (16-65) becomes

$$t_S = \frac{\tau_E + \tau_{ER}}{1 - \alpha\alpha_R} \ln \frac{I_{B1} - I_{B2}}{I_C/h_{FE} - I_{B2}} \tag{16-66}$$

Since $\tau_E = 1.22/\omega_b$ and $\tau_{ER} \approx 1.22/\omega_{bR}$, we obtain a result similar to that obtained by Ebers and Moll,[2] namely,

$$t_s = \frac{1.22(\omega_b + \omega_{bR})}{\omega_b \omega_{bR}(1 - \alpha\alpha_R)} \ln \frac{I_{B1} - I_{B2}}{I_C/h_{FE} - I_{B2}} \tag{16-67}$$

For a uniform-base device, it is reasonable to assume that $\omega_b \approx \omega_{bR}$ and therefore the storage time constant is approximately $2.4/\omega_b(1 - \alpha)$.

If the alloy-type transistor has a graded base such as that found in drift or MADT transistors, then the reverse-cutoff frequency is lowered considerably by the built-in electric field, which is retarding to the flow of carriers. Since $\tau_E = 0.6/\omega_b$ for a graded base in the normal direction, one would conclude that $\tau_{ER} \approx 2.4/\omega_b$ in the reverse direction, since the

reverse base-cutoff frequency is lowered by the same factor that enhances the transit time in the normal direction. With this assumption, the storage-time equation for a diffused-base alloy transistor is, approximately,

$$t_s \approx \frac{3}{\omega_b(1-\alpha)} \ln \frac{I_{B1} - I_{B2}}{I_C/h_{FE} - I_{B2}} \tag{16-68}$$

where ω_b is the base-cutoff frequency in the normal direction and includes the effect of the graded base. Both ω_b and α are measured at the edge of saturation.

For transistors made by single-ended processes such as mesa or planar, the collector resistivity is moderately high and we cannot neglect the τ_{CS} term in Eq. (16-61), since the current I_{Rn} and the stored charge Q_{CS} are appreciable. Because of this effect, the inverse alpha is very low, $\alpha_R \approx 0$. Therefore,

$$\tau_S \approx \tau_E + \tau_{CS} \tag{16-69}$$

wherein it is assumed that the forward alpha is equal to unity. In Eq. (16-69), τ_E is given by $0.6/\omega_b$.

To determine the magnitude of τ_{CS}, we can write that in the collector

$$I_{Rn} \approx \frac{qAD_{nc}n_{pc}\epsilon^{qV_C/kT}}{L_{nc}} \tag{16-70}$$

where L_{nc} is the diffusion length of electrons and is a function of the *minority-carrier lifetime* τ_{nc}. Assuming a linear carrier gradient, the total stored collector charge is (area of triangle)

$$Q_{CS} \approx \frac{qAn_{pc}\epsilon^{qV_C/kT}L_{nc}}{2} \tag{16-71}$$

so that

$$I_{Rn} \approx \frac{2D_{nc}Q_{CS}}{L_{nc}^2} = \frac{Q_{CS}}{\tau_{nc}/2} \tag{16-72}$$

Here we see that the collector time constant is

$$\tau_{CS} = \frac{\tau_{nc}}{2} \tag{16-73}$$

or one-half the minority-carrier lifetime in the collector.

The storage-time equation for mesa- or planar-type structures is

$$t_s \approx \left(\frac{0.6}{\omega_b} + \frac{\tau_{nc}}{2}\right) \ln \frac{I_{B1} - I_{B2}}{I_C/h_{FE} - I_{B2}} \tag{16-74}$$

For low storage time, it is essential that the collector lifetime be made as small as possible. This is usually accomplished in the processing of high-speed switching transistors by the intentional introduction of certain impurities which drastically reduce the collector lifetime. The effectiveness of such lifetime treatments is determined by the measurement of the recovery time of the collector-to-base diode.[10,11]

If the thickness of the collector region is smaller than the minority-carrier diffusion length as is the case for epitaxial transistors, Eqs. (16-70) to (16-74) must be modified accordingly. For epitaxial transistors having an epitaxial collector of thickness W_e in centimeters, it has been determined empirically that

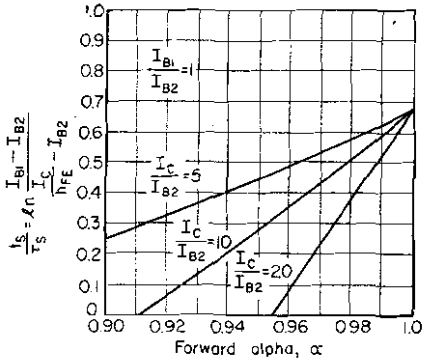


FIG. 16-8. Magnitude of circuit-drive function for storage time t_s.

$$\tau_{CS} \approx \frac{W_e^2}{2} \quad \text{sec} \quad W_e \ll L_{nc} \tag{16-75}$$

Thus, the thickness of the epitaxial layer becomes an important design factor for switching transistors.

All the foregoing expressions for t_s have in common the circuit-drive function given by the logarithmic term. A plot of this function is shown in Fig. 16-8 for different values of the turnoff ratio I_C/I_{B2}. One sees that storage time increases as the transistor h_{FE} gets larger or as the transistor is driven harder. Increasing the magnitude of I_{B2} lowers t_s. It is interesting to note that when h_{FE} is very large, or if $I_{B1} = I_{B2} = I_C$, the circuit-drive function reaches the limiting value of 0.69. This yields the useful relationship

$$t_s \approx 0.7\tau_S \tag{16-76}$$

To close this section it should be pointed out that in saturation the depletion layers of both junctions are very narrow and therefore the

effective base width used in the calculation of ω_b is approximately equal to the physical base width of the transistor.

16-7. Fall Time. The last switching parameter is the fall time t_f, which is the time required for the collector current to decrease to $0.1I_C$. During this interval, the transistor is operating in the active region again, but this region is being traversed in the direction opposite to that of rise time. Therefore, during the fall-time period, the amount of charge to be removed from the base is equal to that which was added during the rise-time interval. For this reason, the charge analysis for

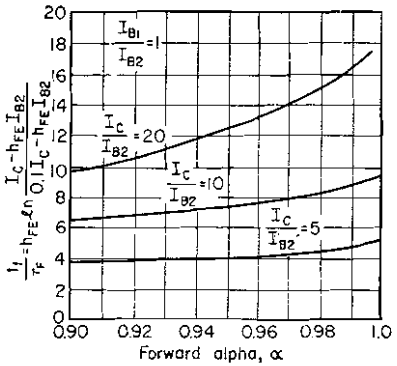


FIG. 16-9. Magnitude of circuit-drive function for fall time t_f.

fall time yields the same time constant as for rise time, given by Eq. (16-45).[3] Therefore, the integral equation (see Eq. 16-30) becomes

$$\int_{I_C}^{0.1I_C} \frac{dI_C}{I_{B2} - I_C/h_{FE}} = \int_0^{t_f} \frac{dt}{1/\omega_T + 1.7R_LC_{T_C}} \tag{16-77}$$

and the integral solution yields

$$t_f \approx h_{FE}\left(\frac{1}{\omega_T} + 1.7R_LC_{T_C}\right) \ln \frac{I_C - h_{FE}I_{B2}}{0.1I_C - h_{FE}I_{B2}} \tag{16-78}$$

The magnitude of the circuit-drive function in Eq. (16-78) is plotted in Fig. 16-9. It is seen that t_f increases with increasing h_{FE}, but primarily decreases as the magnitude of the circuit ratio I_C/I_{B2} decreases.

16-8. Charge-control Parameters of Switching Transistors. In summary, the design of high-speed switching transistors requires that the base-cutoff frequency be as large as possible and that the emitter and collector junction capacitances be as small as possible. Furthermore, to minimize charge storage in the collector, the minority-carrier concentration and/or lifetime should be made as low as possible. These requirements come as a result of the charge analysis of the grounded-emitter switching transistor which yields expressions for the delay, rise, storage,

and fall times. For maximum switching speed, the magnitudes of the delay-plus-rise times (t_{ON}) and the storage-plus-fall times (t_{OFF}) must be small. Present transistor technology makes possible devices having total switching times in the range of 10 to 100 nsec (nanoseconds, 10^{-9} sec). Fig. 16-10 provides typical switching data for a high-speed n-p-n silicon epitaxial transistor. The curves give the values of t_{ON} and t_{OFF} for different levels of collector current and circuit ratio I_C/I_{B1}.

One useful way of satisfying the circuit designer's problem of predicting the switching times of a particular device for circuit-drive conditions,

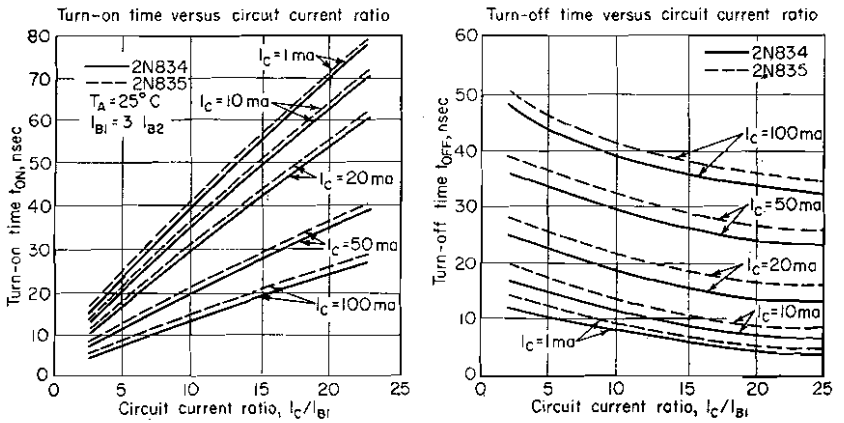


FIG. 16-10. Typical switching characteristics as functions of circuit current ratio for a 2N834 n-p-n silicon epitaxial planar transistor. (*Courtesy of Motorola, Inc.*)

different from that specified by the manufacturer, is to provide data on the so-called charge-control parameters of the transistor.[3,12] These charge-control parameters are Q_{OFF}, τ_R, τ_S, and τ_F; they manifest themselves when the various switching-time expressions are written in the form

$$t_d = \frac{Q_{OFF}}{I_{B1}} \tag{16-79}$$

$$t_r = \tau_R h_{FE} \ln \frac{h_{FE}I_{B1}}{h_{FE}I_{B1} - 0.9I_C} \tag{16-80}$$

$$t_s = \tau_S \ln \frac{I_{B1} - I_{B2}}{I_C/h_{FE} - I_{B2}} \tag{16-81}$$

$$t_f = \tau_F h_{FE} \ln \frac{I_C - h_{FE}I_{B2}}{0.1I_C - h_{FE}I_{B2}} \tag{16-82}$$

In each of the above equations, we see that the charge-control parameter is multiplied by a circuit-drive function. In fact, Figs. 16-6, 16-8, and 16-9 are plots of t_r/τ_R, t_s/τ_S, and t_f/τ_F, respectively.

From the theory of the previous sections, we can write

$$Q_{OFF} \approx 2C'_{Tc}V_{BE(OFF)}^{1/2} \qquad V_{CC} \gg V_{BE(OFF)} \tag{16-83}$$

$$\tau_R \approx \tau_F \approx \frac{1}{\omega_T} + 1.7R_LC_{Tc} \tag{16-84}$$

$$\tau_S \approx \frac{2.4}{\omega_b(1-\alpha)} \quad \text{uniform base alloy}; \quad \omega_b = \omega_{bR};\ \alpha_R = 1 \tag{16-85}$$

$$\tau_S \approx \frac{3}{\omega_b(1-\alpha)} \quad \text{graded base alloy}; \quad \omega_b \approx 4\omega_{bR};\ \alpha_R = 1 \tag{16-86}$$

$$\tau_S \approx \frac{0.6}{\omega_b} + \frac{\tau_{nc}}{2} \quad \text{single-ended types}; \quad \alpha_R \approx 0 \tag{16-87}$$

The above relations provide a reasonably accurate means of calculating the magnitudes of the charge-control parameters from the physical properties of the device structure. On the other hand, any attempt to determine the charge-control parameters from measurements of ω_T, ω_b, α, ω_{bR}, etc. would be exceedingly difficult, since these parameters must be measured at the edge of saturation. Therefore, a means of measuring Q_{OFF}, τ_R, τ_S, τ_F directly becomes paramount. Several methods of measurement have been proposed, the details of which are covered in the references.[3,13,14] However, the technique is based on the principle that the circuit-drive functions converge to a limiting value when I_{B1} is made at least five times greater than I_C/h_{FE}. For example, if $I_{B1} = 5I_C/h_{FE}$, the storage-time circuit-drive function becomes approximately ln 2. By setting up such circuit conditions and measuring t_s, we have

$$\tau_S \approx \frac{t_s}{\ln 2} \tag{16-88}$$

Thus, by providing measured data as to how Q_{OFF} varies with $V_{BE(OFF)}$ and how τ_R, τ_S, and τ_F vary with current, the designer is equipped with a means for calculating the switching times for any set of circuit-drive conditions.[13] It should be apparent that both τ_R and τ_F are also functions of the collector supply voltage V_{CC}, since this determines the magnitude of R_LC_{Tc} at a fixed I_C.

PROBLEMS

16-1. Measurements of a 2N705 p-n-p germanium mesa transistor indicate that $C_{Tc} = 3.5$ $\mu\mu f$ at 2 volts, $C_{Tc} = 5$ $\mu\mu f$ at 10 volts, $f_T \approx f_{\alpha b} = 250$ megacycles and $h_{FE} = 40$ at $V_{CE} = -0.3$ volt, $I_C = -10$ ma. The collector-region lifetime is determined to be 0.12 μsec. For this device, calculate t_d, t_r, t_s, and t_f in a switching circuit in which $I_C = -10$ ma, $I_{B1} = -1$ ma, $I_{B2} = 0.25$ ma, $V_{CC} = -3.5$ volts, $V_{BE(OFF)} = 1.25$ volts, and $R_L = 300$ ohms.

16-2. Calculate the storage time t_s for a 2N706 n-p-n silicon mesa transistor which has a 2-ohm-cm epitaxial collector region with a thickness of 10 μ and a lifetime of 0.02 μsec. The base time constant is such that the excess base charge is negligible. Use a circuit in which $I_C = I_{B1} = -I_{B2} = 10$ ma.

16-3. An n-p-n germanium-alloy switching transistor is designed with equal emitter and collector areas of 100 mil^2. The base region is 1 ohm-cm p type and is 0.5 mil thick, resulting in a 50-ma beta of 100 near saturation. Calculate the rise and fall times in a circuit for which $I_C = 50$ ma, $I_{B1} = 5$ ma, $I_{B2} = -1$ ma, and $R_L = 500$ ohms.

16-4. The charge-control parameters of a 2N501 p-n-p germanium MADT transistor are measured at $V_{CC} = -3.5$ volts. They are: $Q_{OFF} = 25$ $\mu\mu$coulombs at $V_{BE(OFF)} = 1.25$ volts, $\tau_R = \tau_F = 3$ mμsec at $I_C = -10$ ma, and $\tau_S = 55$ mμsec at $I_{BX} = 0.6$ ma. For this device, $h_{FE} = 25$ at $I_C = -10$ ma. From this data, calculate t_d, t_r, t_s, and t_f in the switching circuit given in Prob. 16-1.

REFERENCES

1. Anderson, A. E.: Transistors in Switching Circuits, *Proc. IRE*, vol. 40, pp. 1541–1548, November, 1952.
2. Moll, J. L.: Large-signal Transient Response of Junction Transistors, *Proc. IRE*, vol. 42, pp. 1773–1784, December, 1954.
3. Beaufoy, R., and J. J. Sparkes: The Junction Transistor as a Charge-controlled Device, *ATE J.*, vol. B, pp. 310–327, October, 1957.
4. Baker, A. N.: Charge Analysis of Transistor Operation, *Proc. IRE*, vol. 48, pp. 949–950, May, 1960.
5. Ekiss, J. A., and C. D. Simmons: Calculation of the Rise and Fall Times of an Alloy Junction Transistor Switch, *Proc. IRE*, vol. 48, pp. 1487–1488, August, 1960.
6. Cho, Y.: Calculation of the Rise and Fall Times in the Alloy Junction Transistor Switch Based on the Charge Analysis, *Proc. IRE*, vol. 49, pp. 636–637, March, 1961.
7. Severin, Ernest: Switching Time Formulae for Single-diffused Mesa Transistors, *Semiconductor Prods.*, pp. 37–42, June, 1961.
8. Easley, J. W.: The Effect of Collector Capacity on the Transient Response of Junction Transistors, *IRE Trans.*, vol. ED-4, pp. 6–14, January, 1957.
9. Simmons, C. D.: Hole Storage Delay Time and Its Prediction, *Semiconductor Prods.*, pp. 14–18, May/June, 1958.
10. Lax, Benjamin, and S. R. Neustadter: Transient Response of a p-n Junction, *J. Appl. Phys.*, vol. 25, pp. 1148–1154, September, 1954.
11. Grinich, V. H., and R. N. Noyce: Switching Time Calculations for Diffused Base Transistors, *IRE Wescon Convention Record*, part 3, Electron Devices, pp. 141–147, August, 1958.
12. Sparkes, J. J.: A Study of the Charge-control Parameters of Transistors, *Proc. IRE*, vol. 48, pp. 1696–1705, October, 1960.
13. Simmons, C. D.: High-speed Switching Transistors, *Elec. Design News*, pp. 39–47, September, 1960.
14. Hwang, Y. C., D. S. Cleverley, and D. J. Monsour: Transistor Switching Speed from Base Storage Charges and Their Lifetimes, *Electronic Design*, part I, pp. 52–55, March, 1961, part II, pp. 50–53, April, 1961.