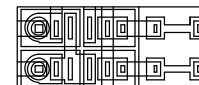
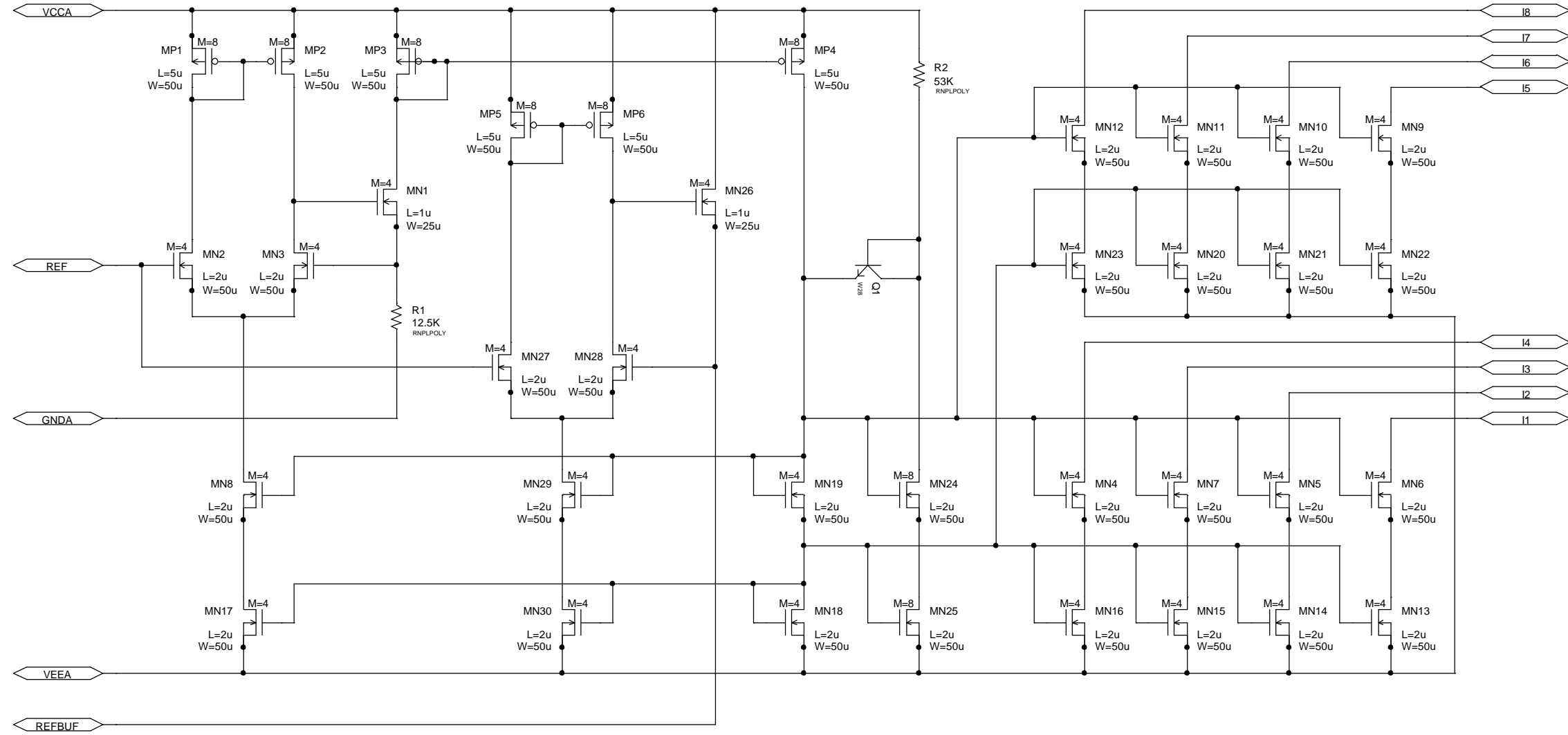
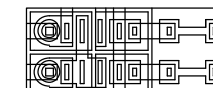
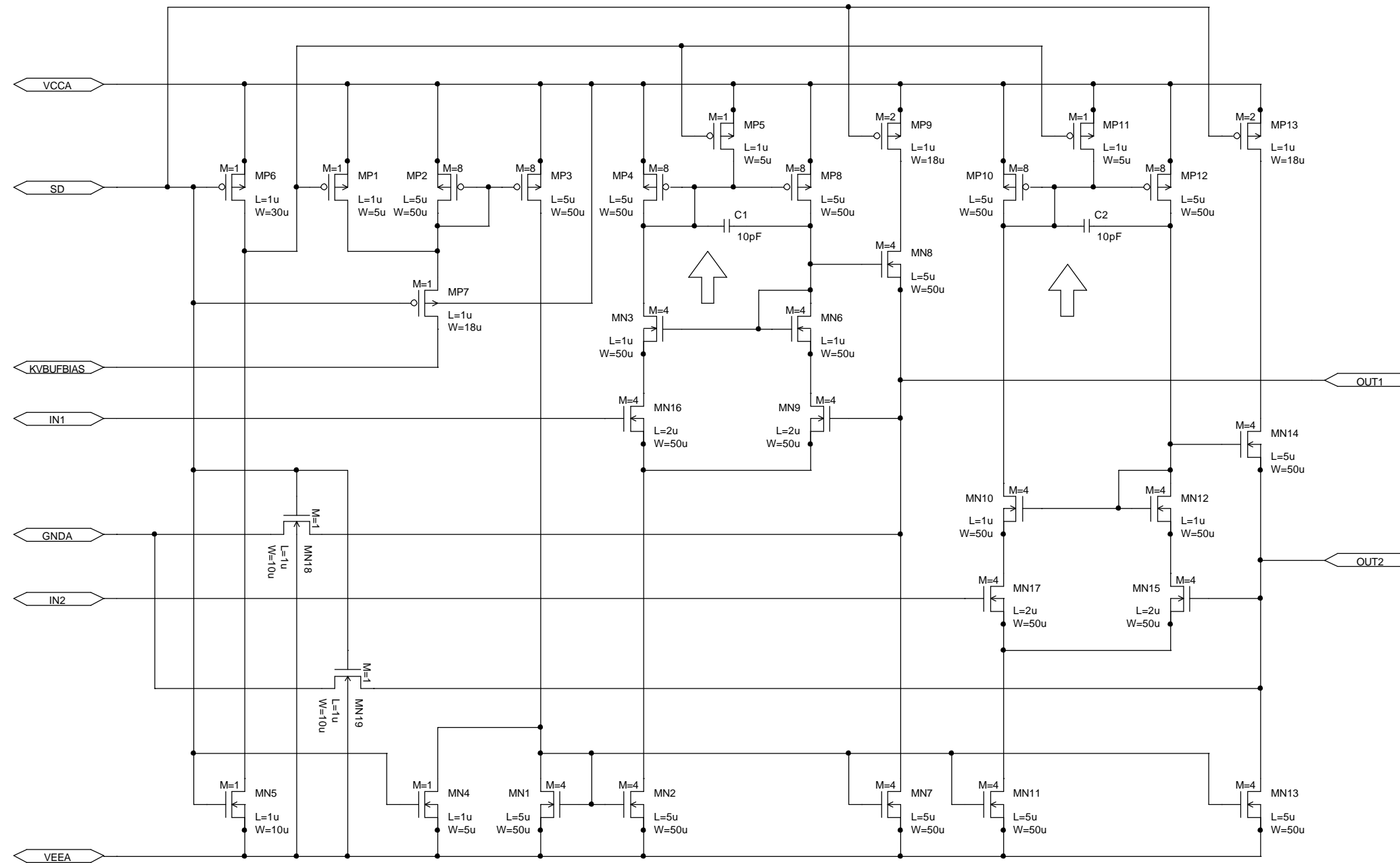


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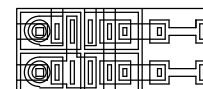
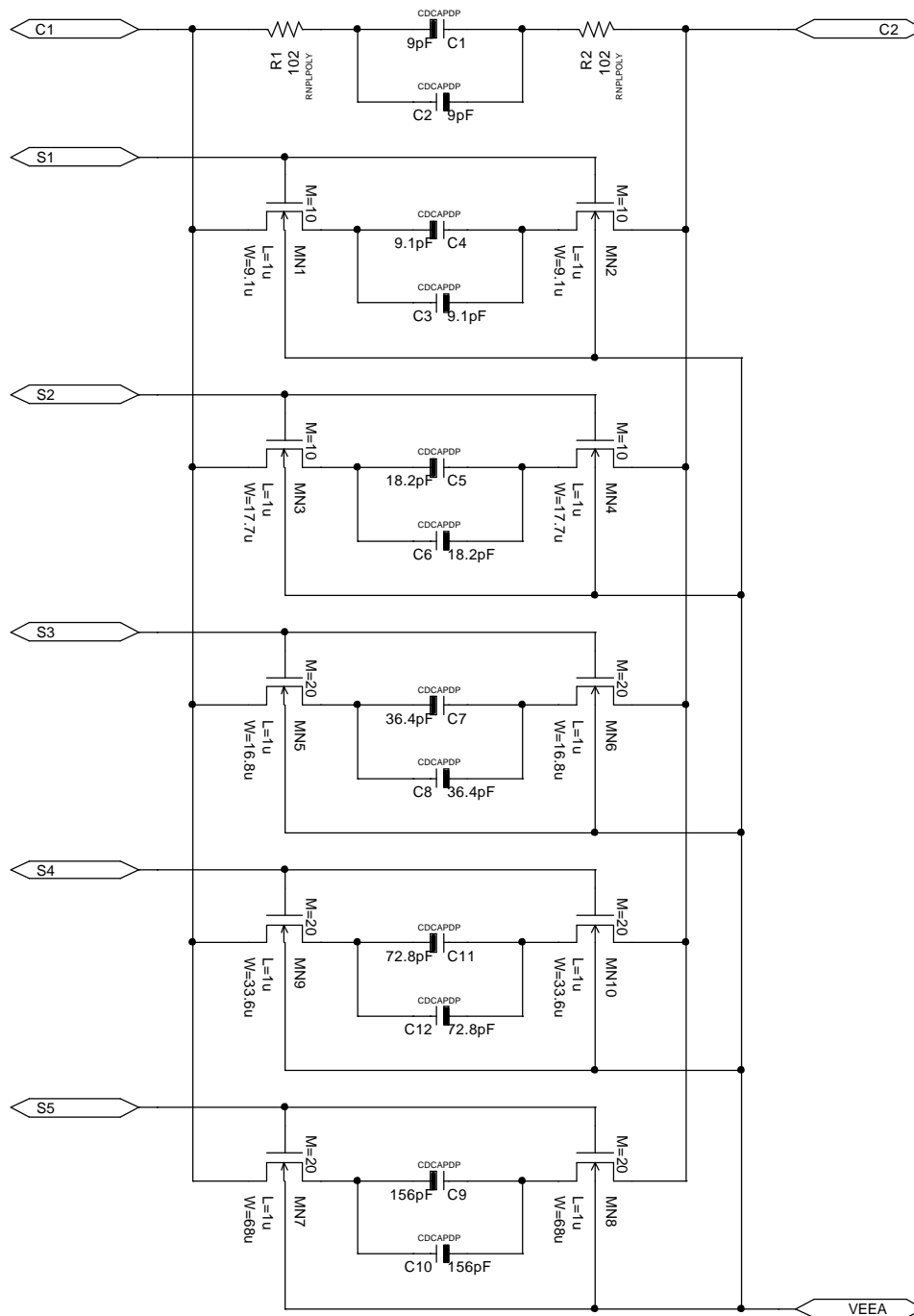
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Title:		REV
Main Bias Generator... RevK, Added Buffer for DAC's		K
Size	FileName:	
B	...BiasGen-RevK.sch	
June 7, 2002, 4:47 PM		Sheet 1 of 1



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Title: Kelvin-Varley DAC Buffer		REV A
Size B	FileName: ...\Buffer-K-V-Cell.sch	
July 28, 2003, 8:37 AM		Sheet 1 of 1



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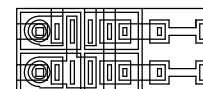
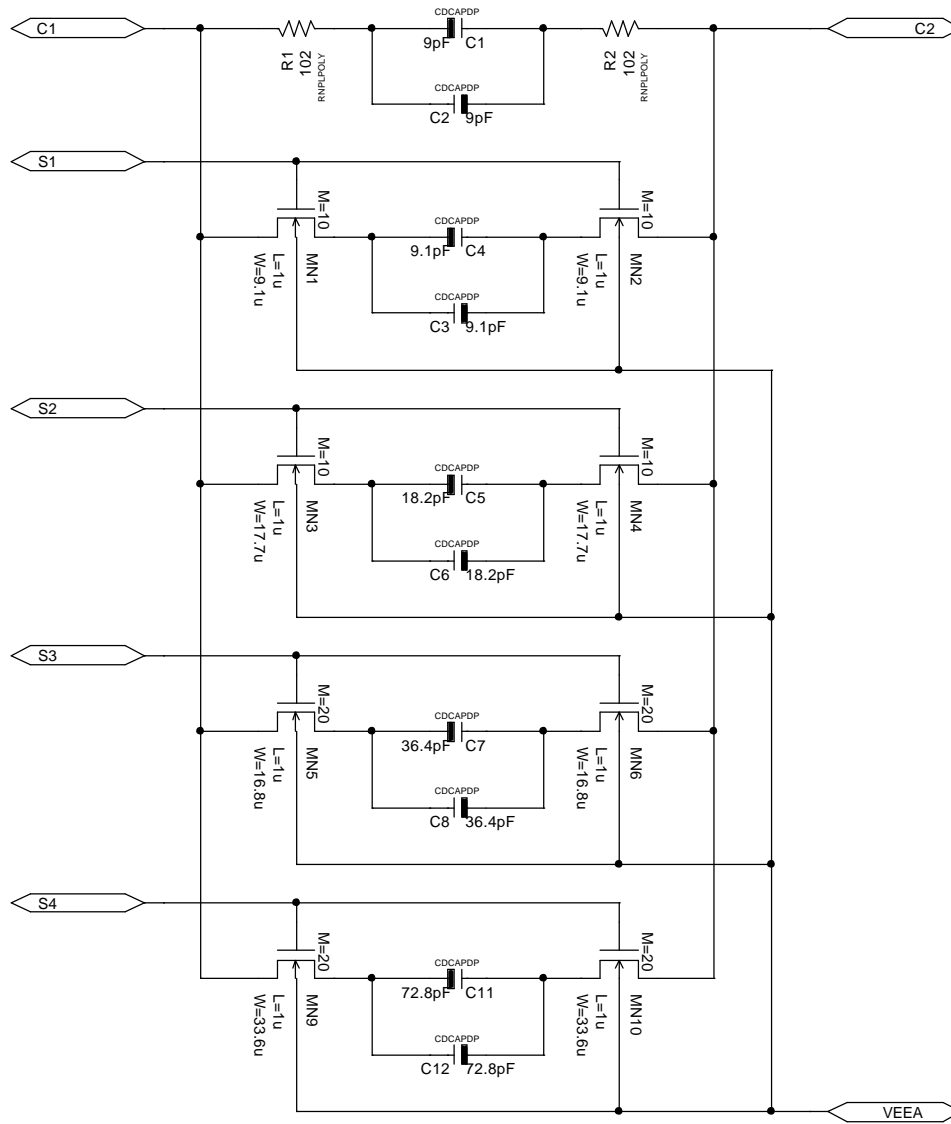
Title:
 Capacitor Module for 1st Main Filter...CAPMOD1...Rev B

Size A
 File Name:
 ...CapModule1stMainRevB.sch

REV
 B

August 15, 2002, 1:34 PM

Sheet 1 of 1



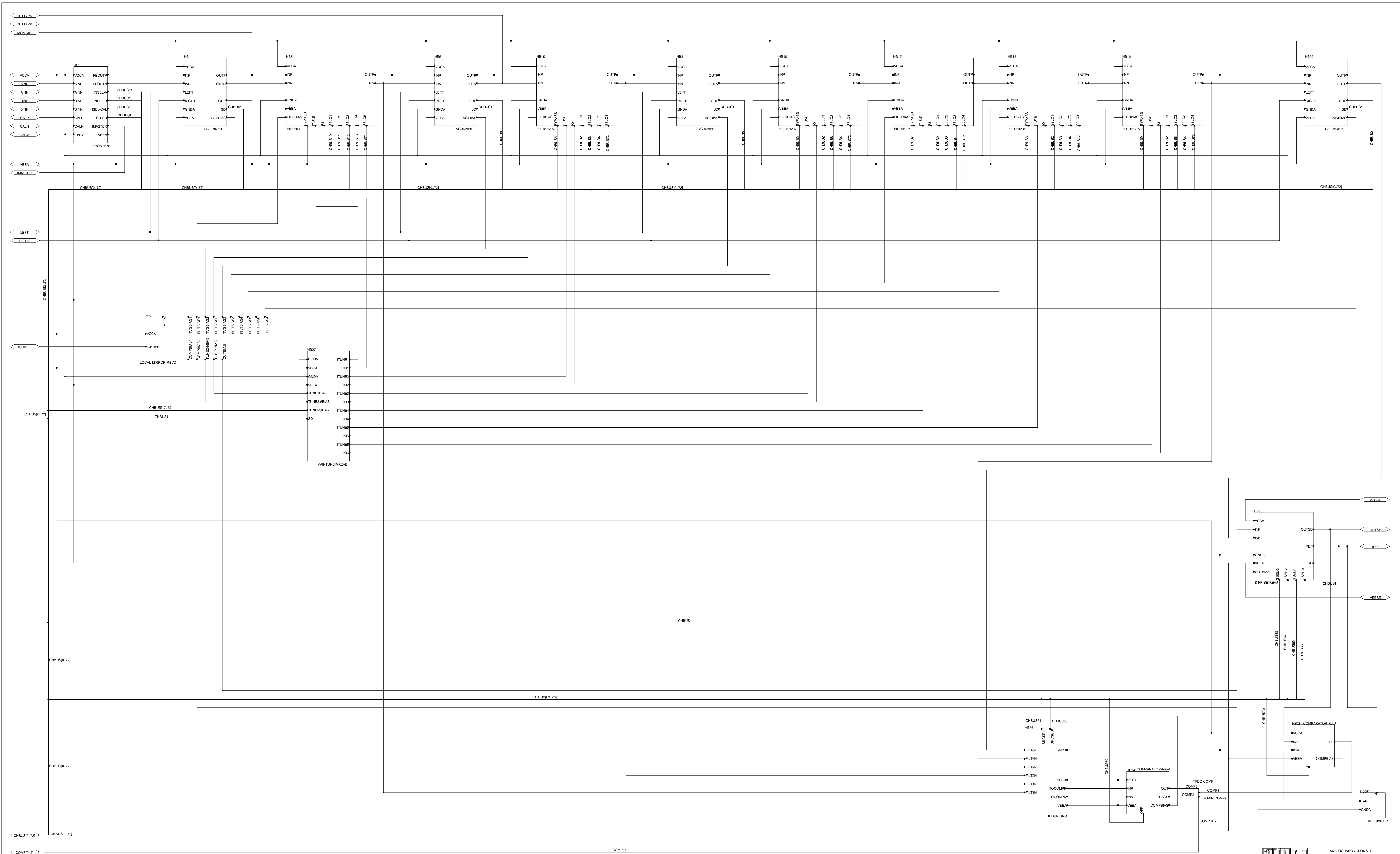
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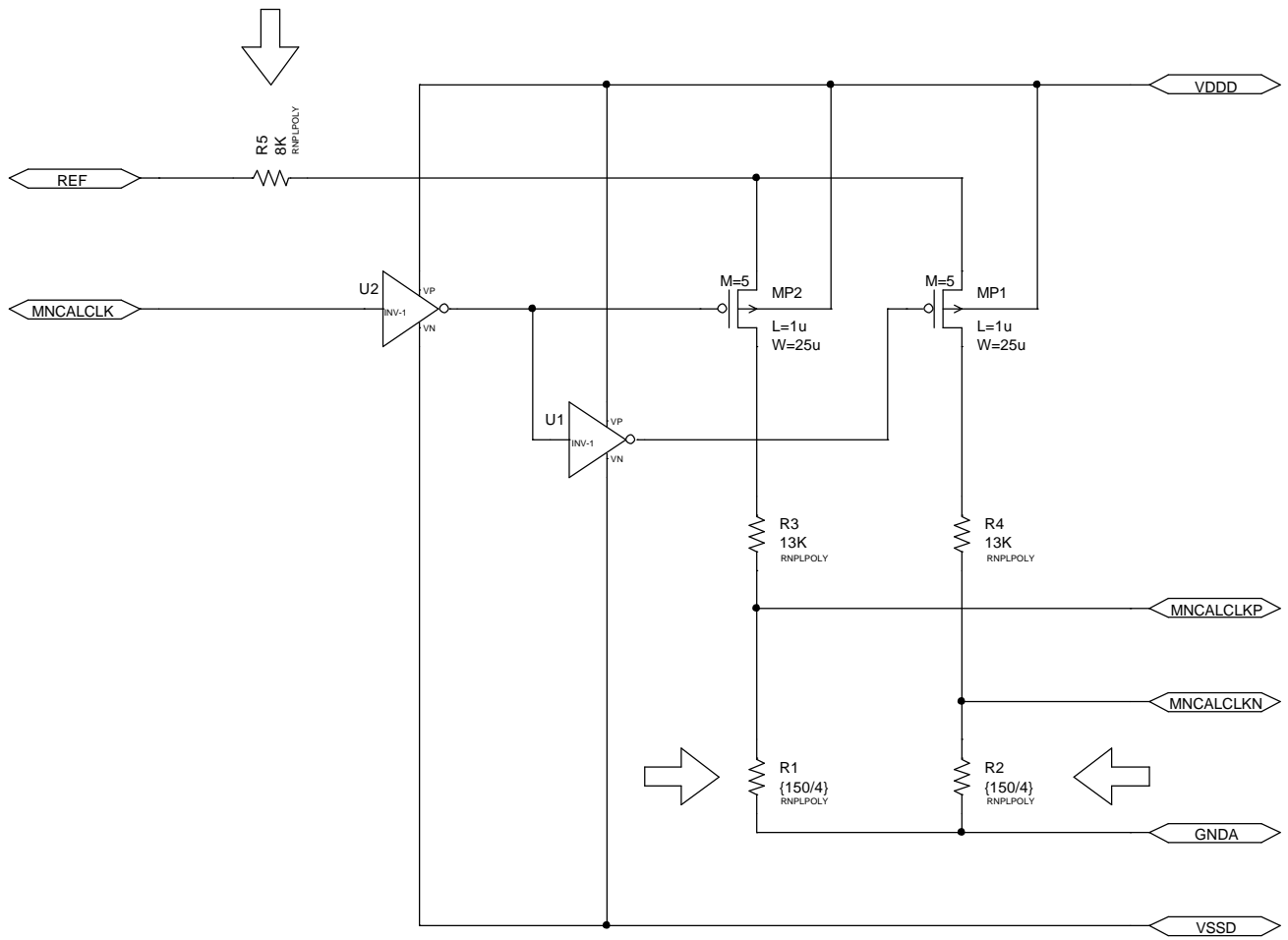
Title:
 Capacitor Module for 1st Main Filter...CAPMOD2-6...Rev C

Size A	FileName: ...\\CapModule2-6MainRevC.sch	REV C
-----------	--------------------------------------------	----------

August 15, 2002, 1:34 PM

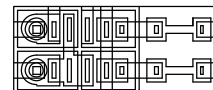
Sheet 1 of 1





➔ INDICATES CHANGES

{150/4} INDICATES 4x 150 ohm in PARALLEL



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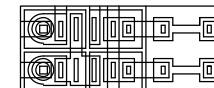
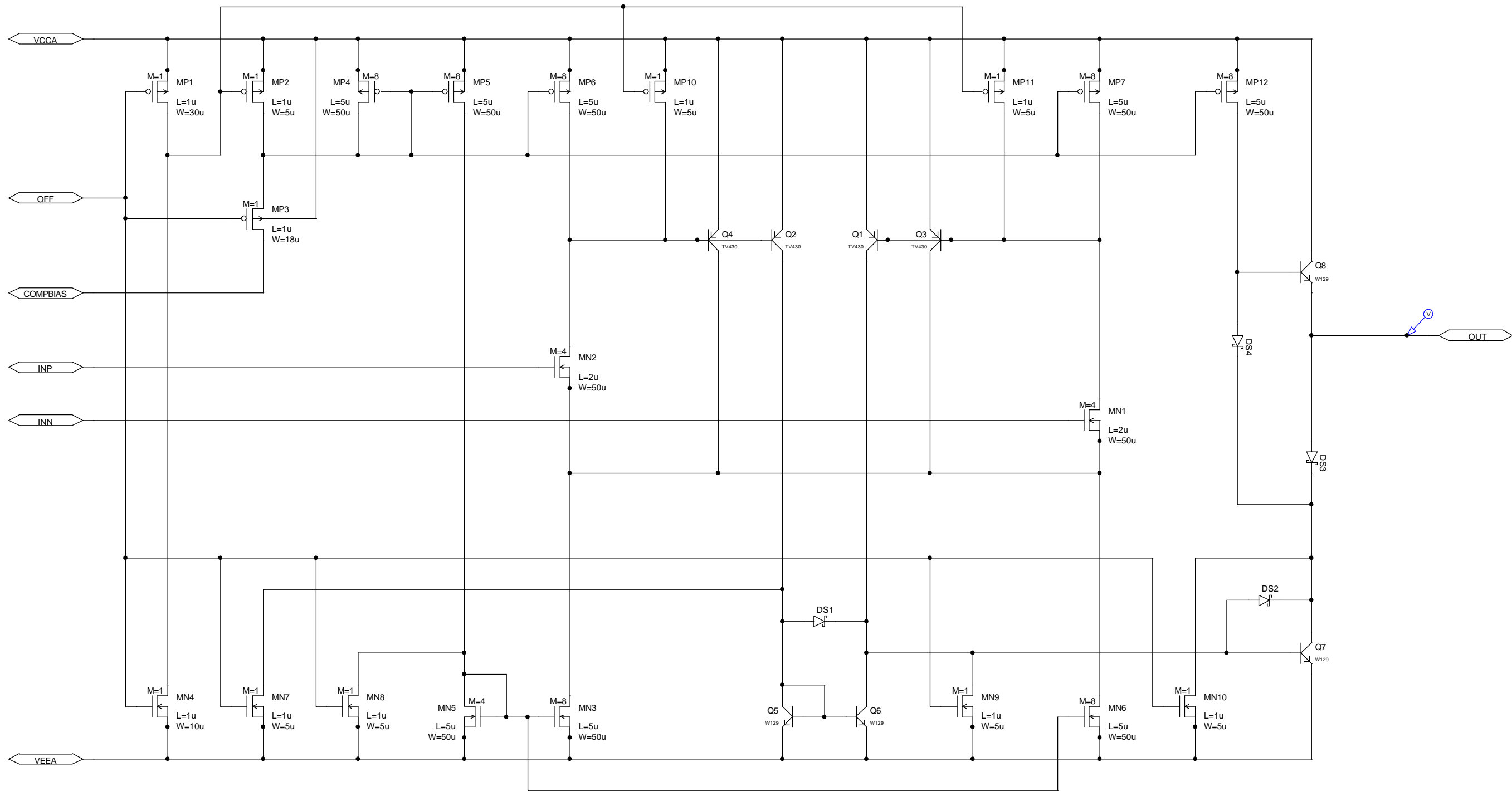
Title:
 CMOS-to-MainCal Interface... Revised for Gain Calibration

Size A
 FileName: ...CMOS-to-MNCAL.sch

REV
 A

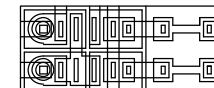
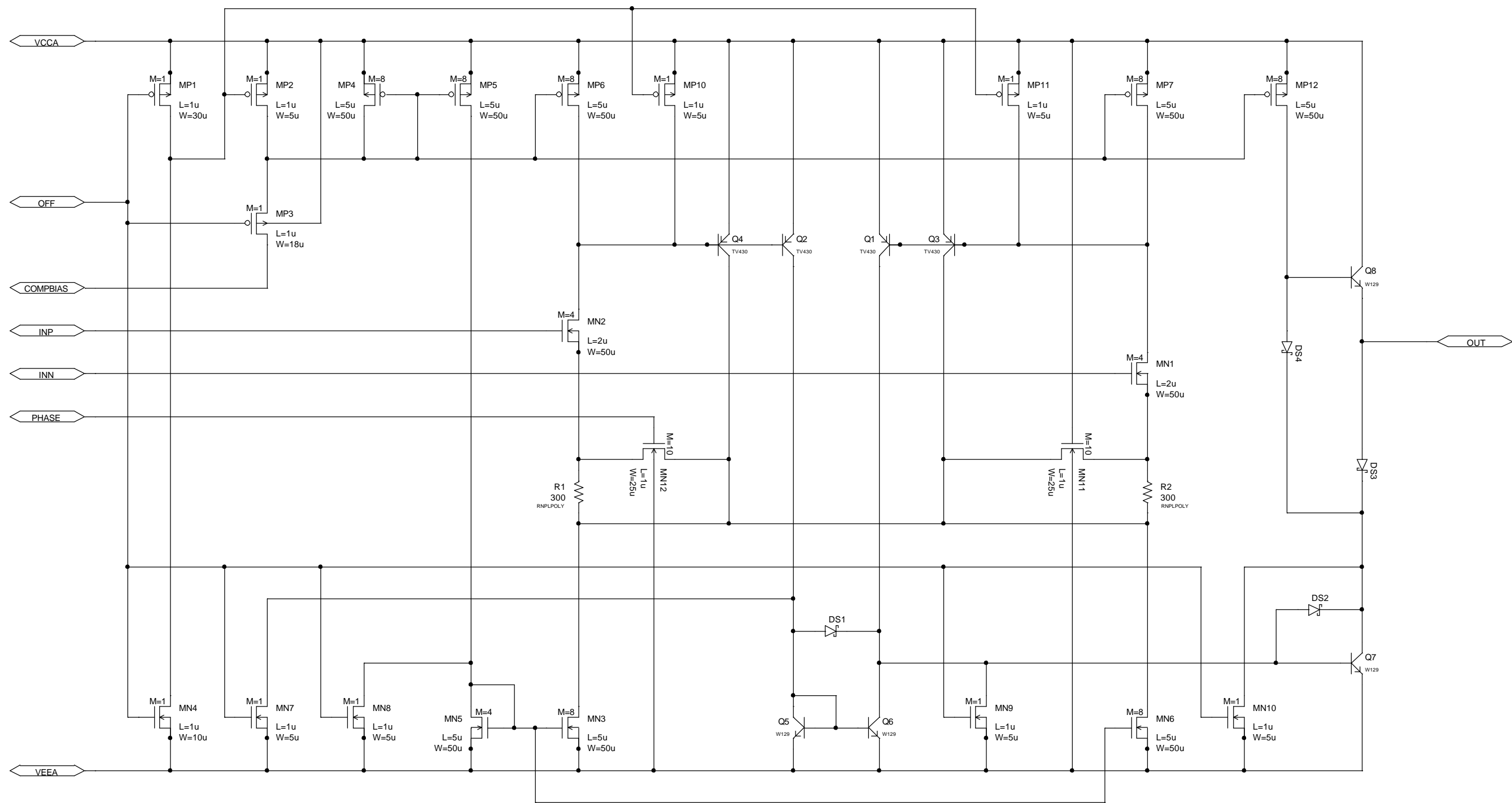
August 22, 2002, 10:25 AM

Sheet 1 of 1



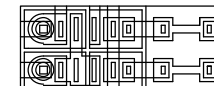
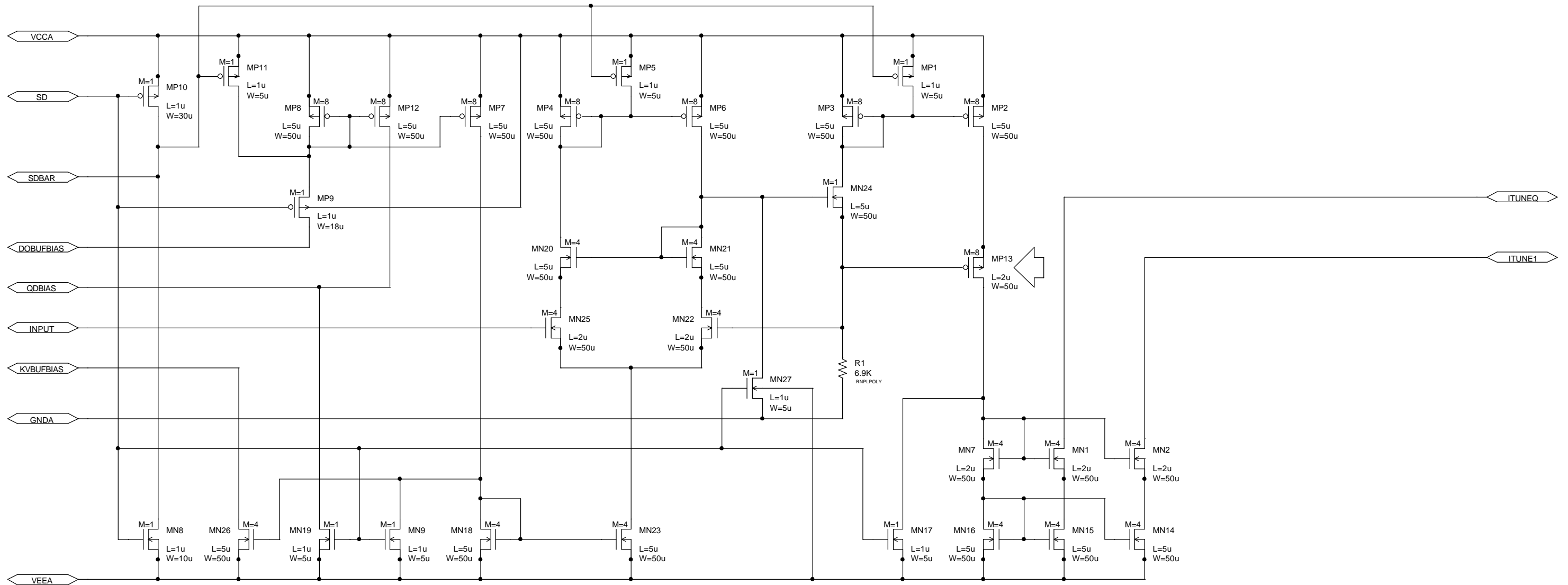
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Title: Comparator (Phase and Amplitude)		
Size B	FileName: ...Comparator-RevJ.sch	REV J
May 1, 2002, 4:01 PM		Sheet 1 of 1



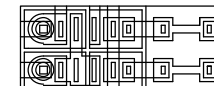
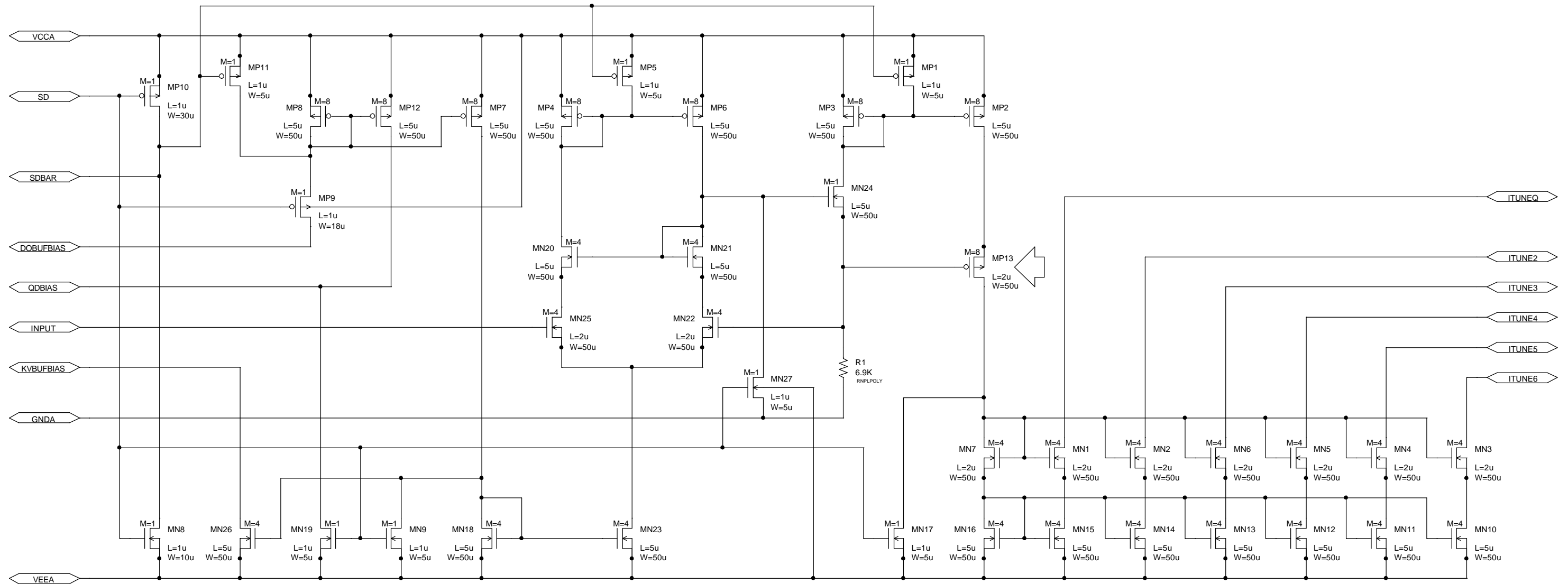
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Title: Amplitude/Phase Comparator		REV K
Size B	FileName: ...Comparator-RevK.sch	
August 22, 2002, 5:02 PM		Sheet 1 of 1



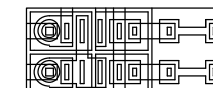
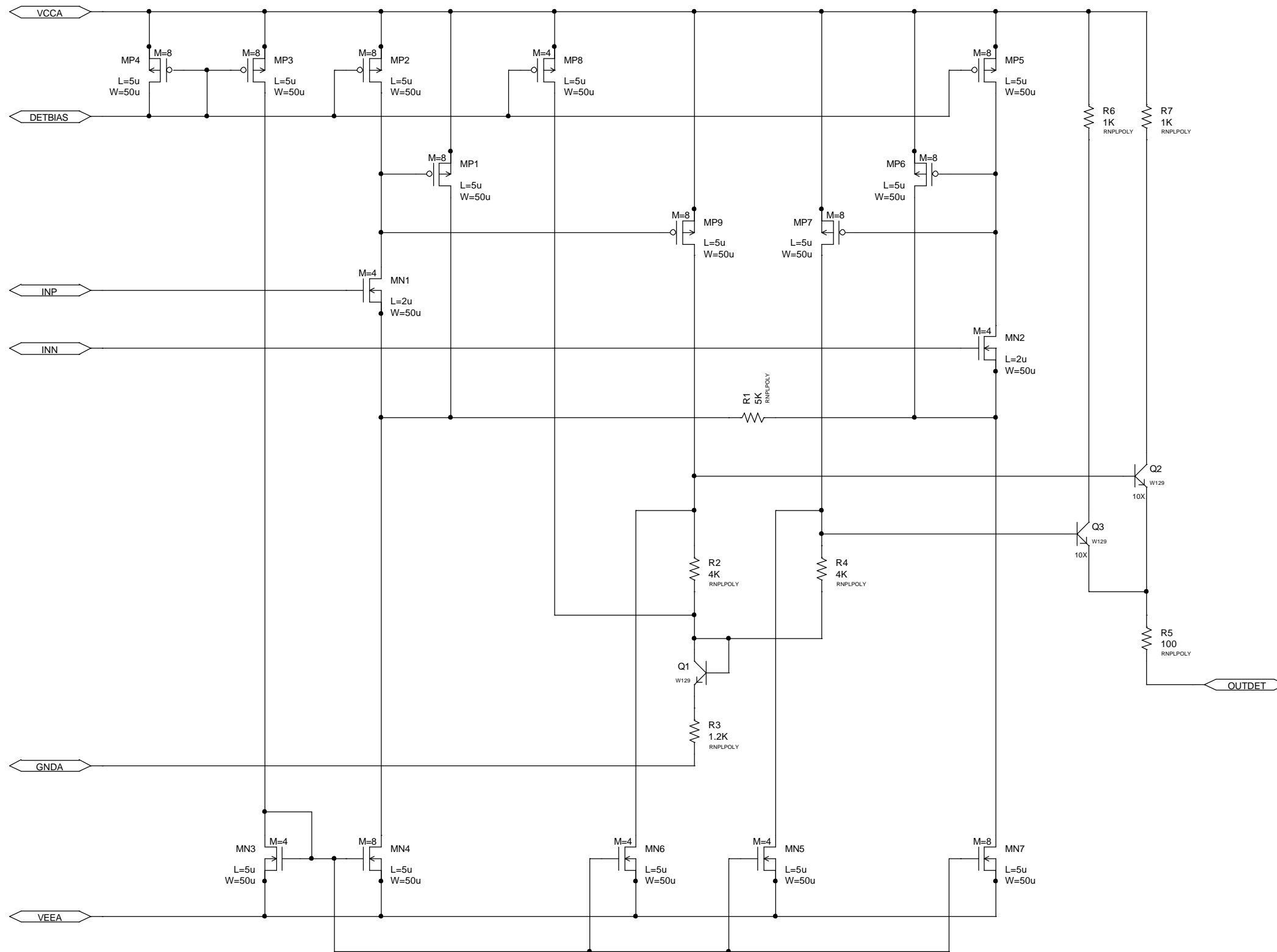
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Title: DAC Output Buffer... 1 Output		REV B
Size B	FileName: ...DAC-OUT-BUF-1Port.sch	REV B
June 2, 2002, 10:08 AM	Sheet 1 of 1	



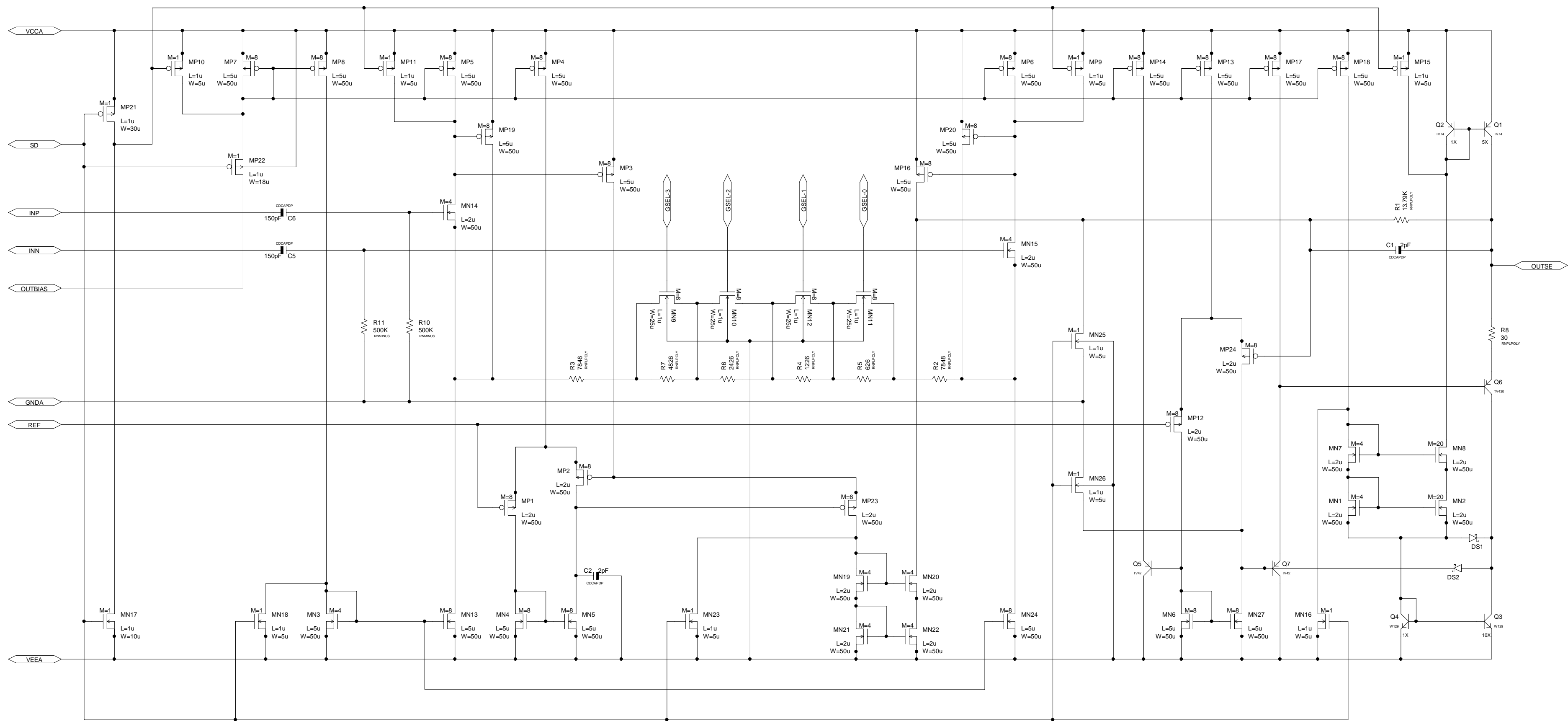
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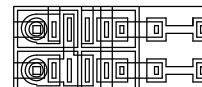
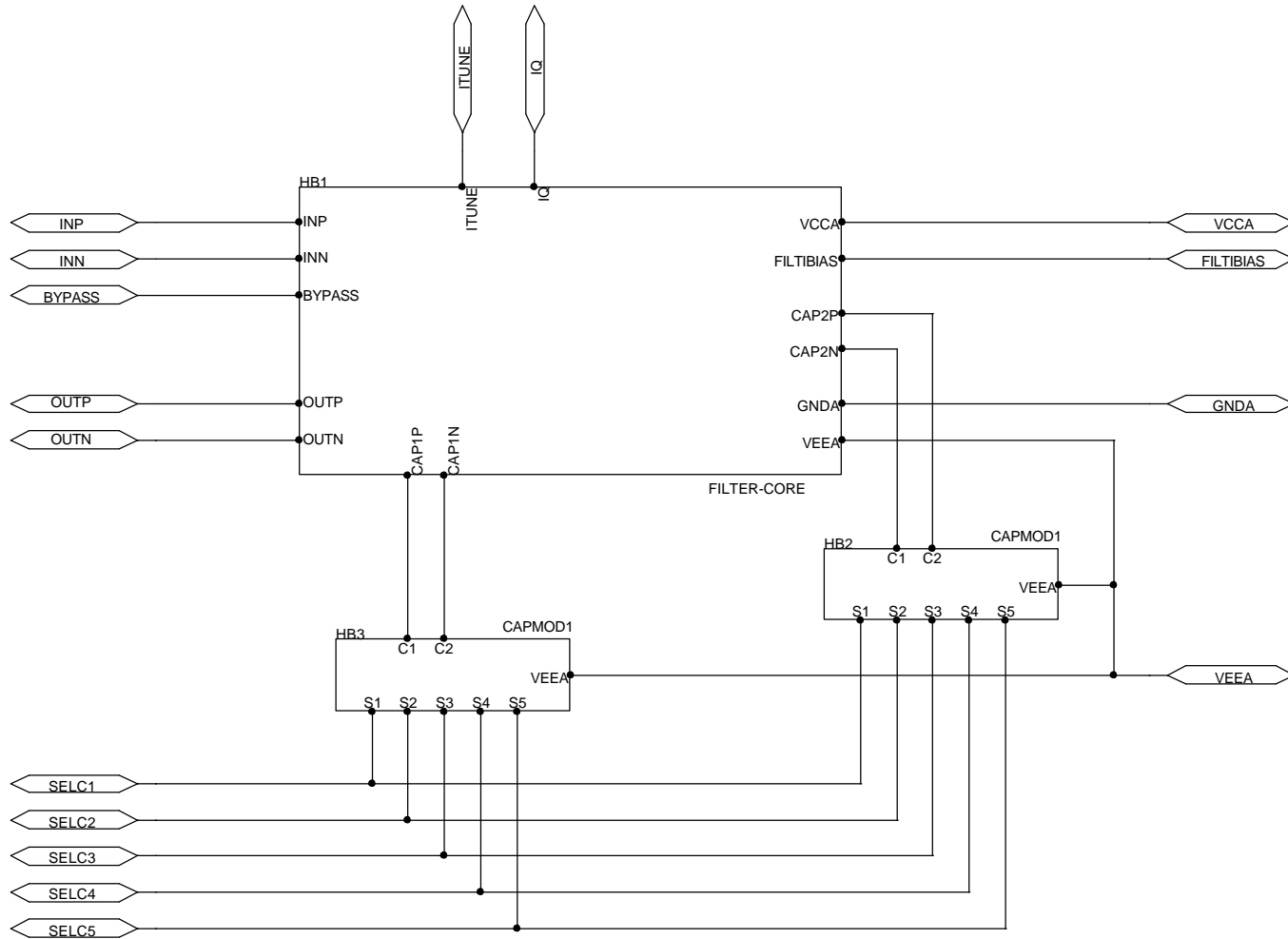
Title: DAC Output Buffer... 5 Outputs		REV B
Size B	FileName: ...DAC-OUT-BUF-5Port.sch	
June 2, 2002, 10:08 AM		Sheet 1 of 1



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Title: Detector		REV J
Size B	FileName: ...Detector-RevJ.sch	
May 2, 2002, 10:02 AM	Sheet 1 of 1	





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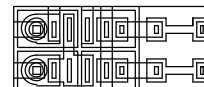
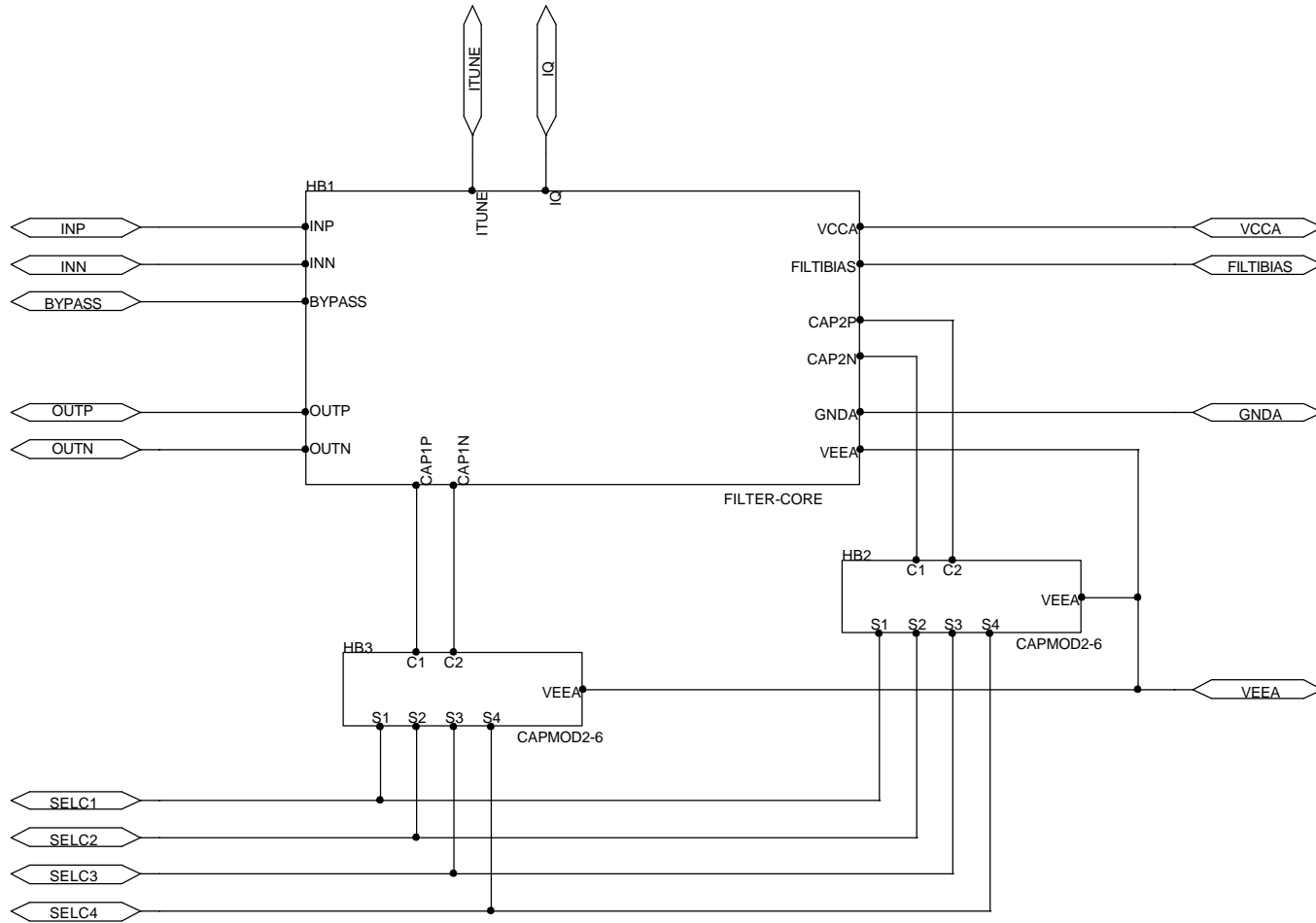
Title:
 Filter 1st Main

Size A FileName:
 ...Filter1stMain-RevB.sch

REV
 B

September 8, 2002, 12:05 PM

Sheet 1 of 1



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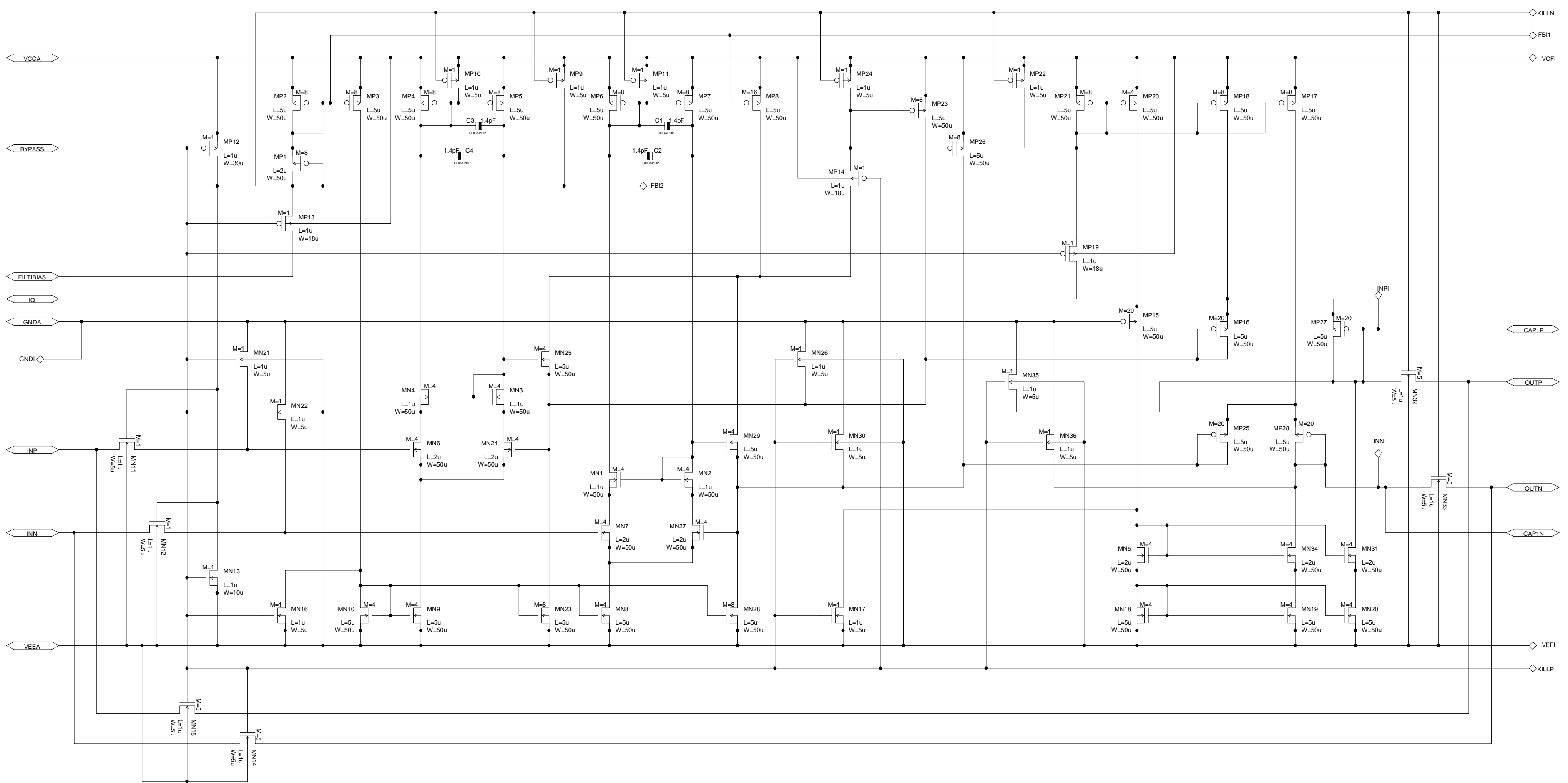
Title:
 Filters 2-6

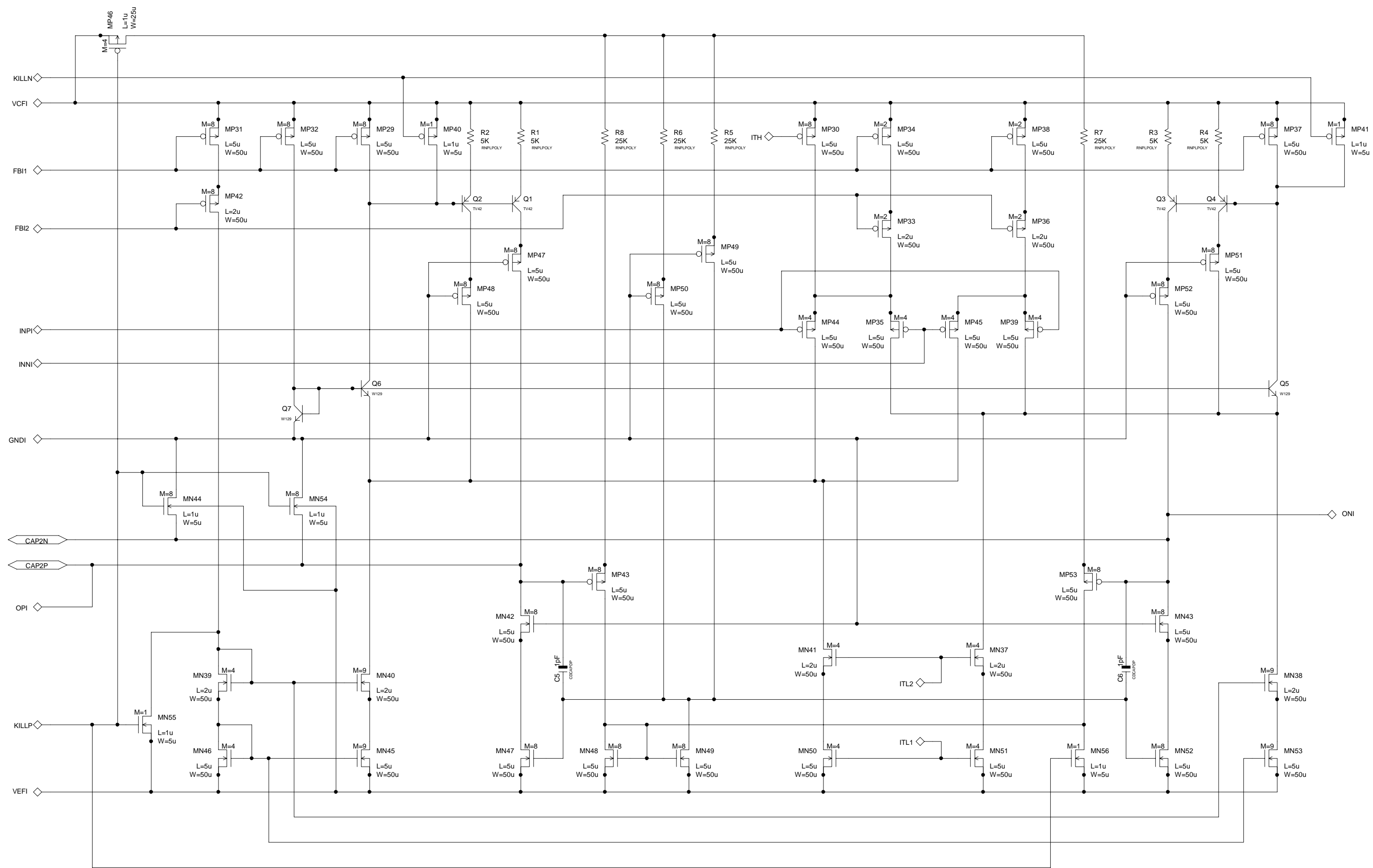
Size A FileName:
 ...Filter2-6Main-RevB.sch

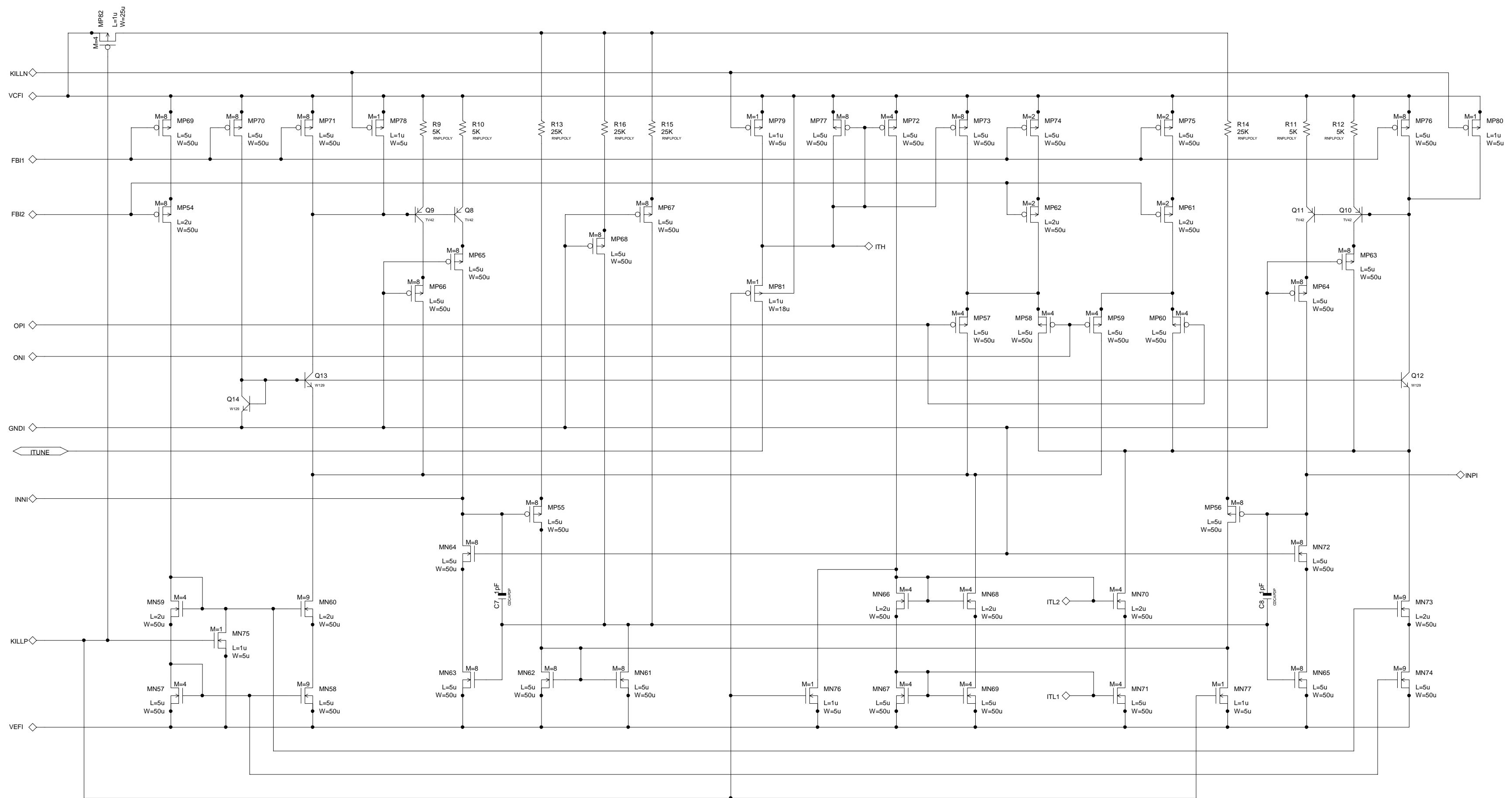
REV
 B

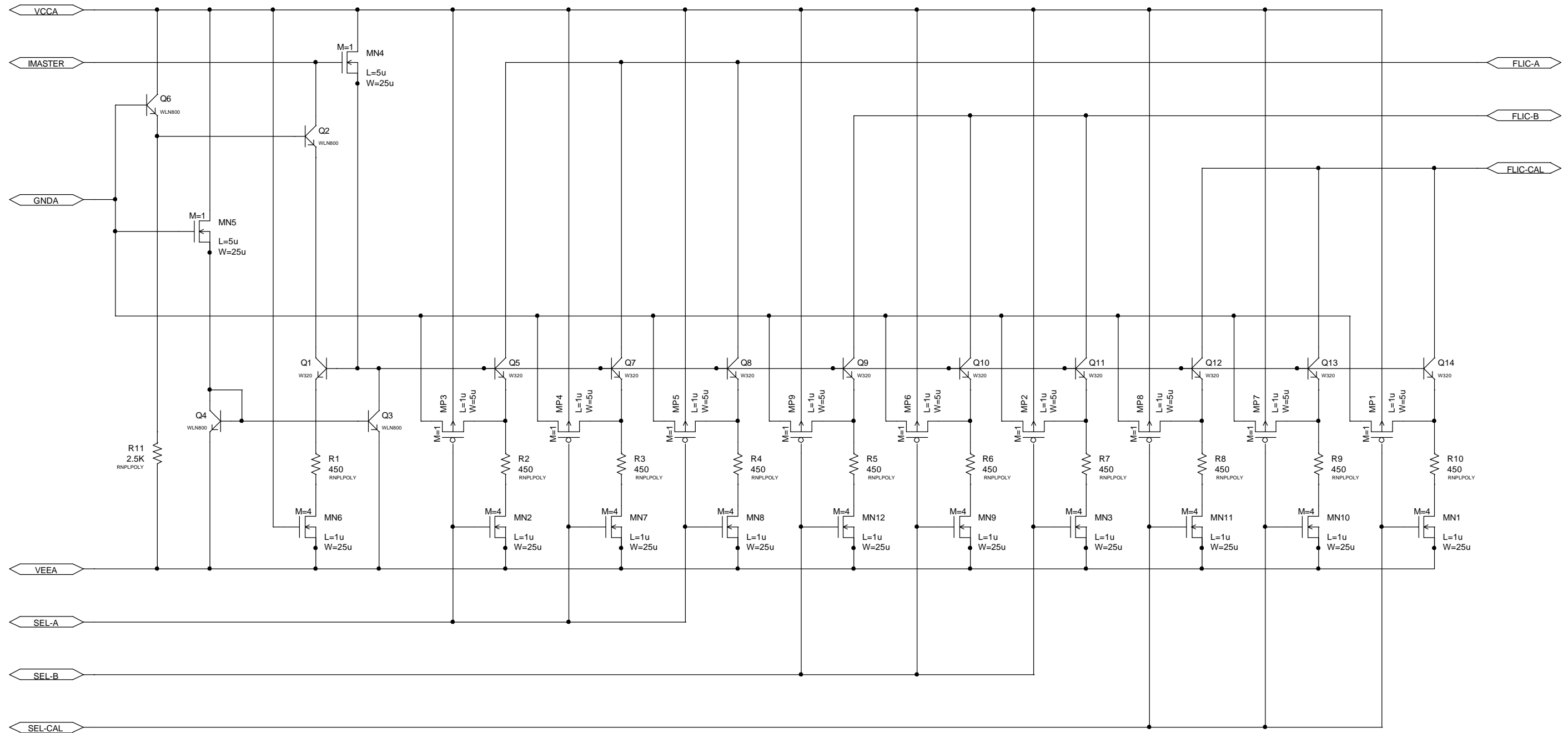
September 8, 2002, 12:10 PM

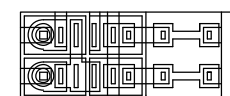
Sheet 1 of 1

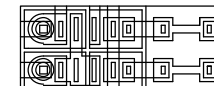
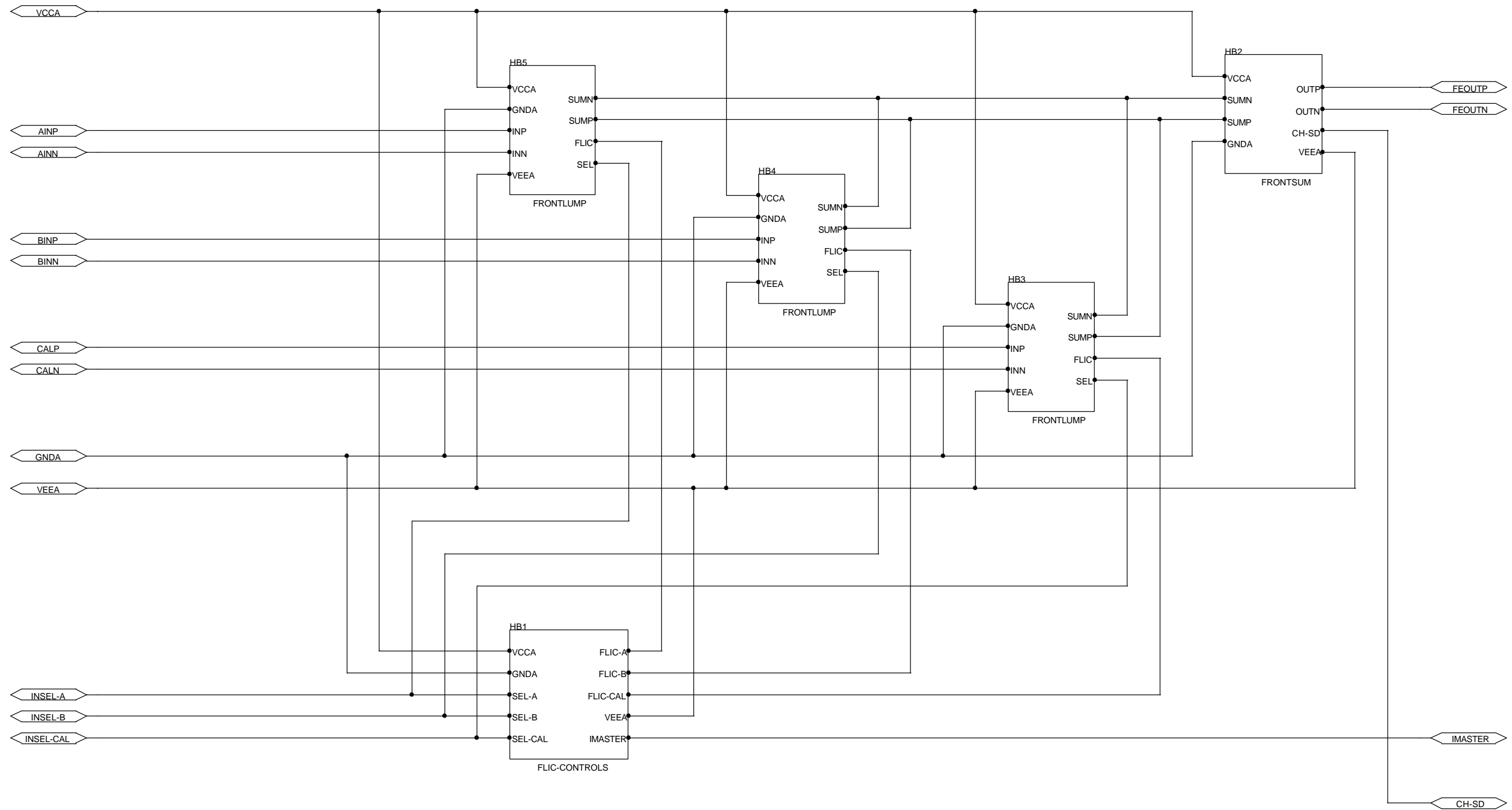






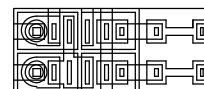
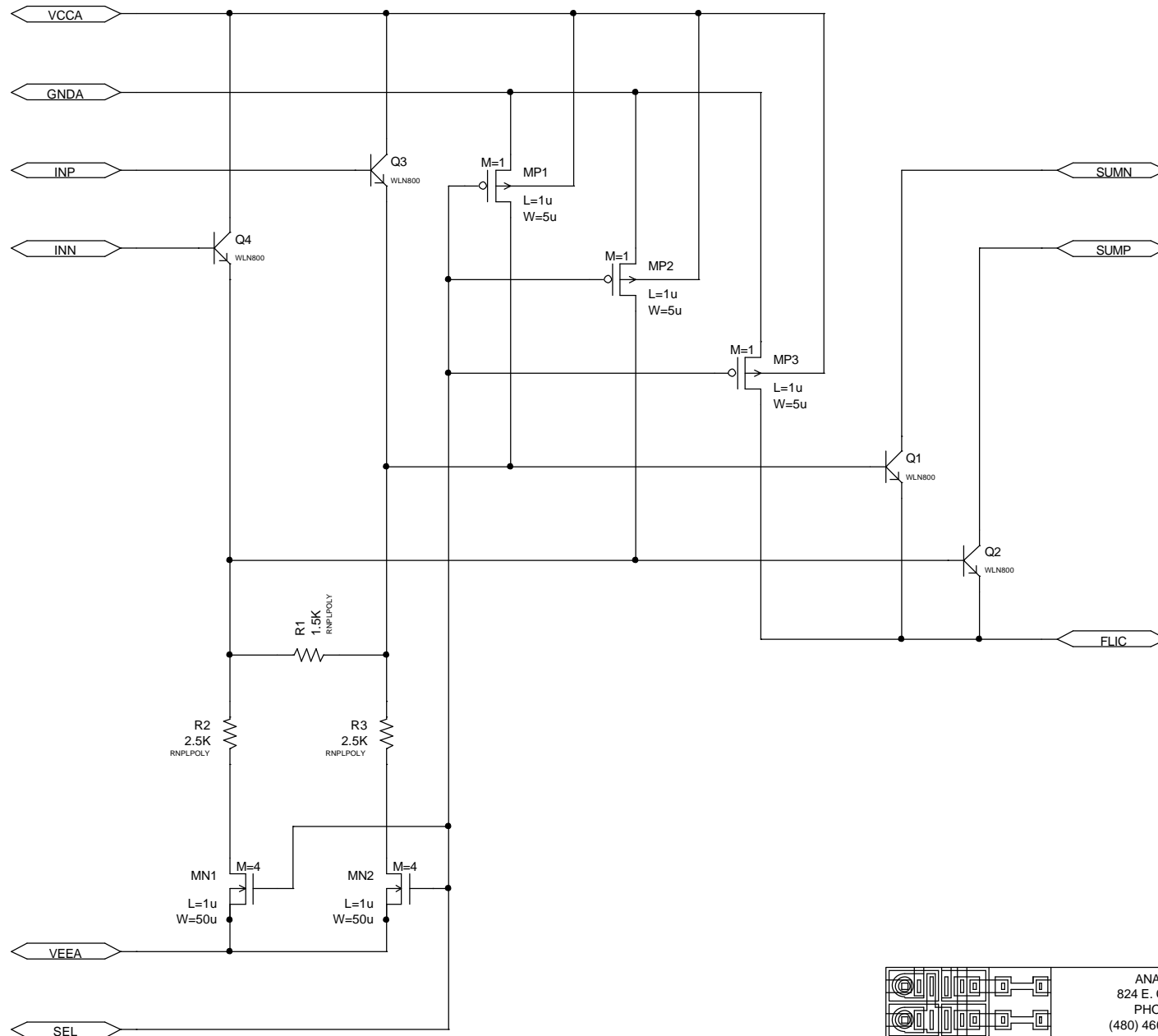


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Title: FLIC Controls			
Size: B	FileName: ...\\FLIC-Controls.sch	REV: J	
May 2, 2002, 9:55 AM		Sheet 1 of 1	



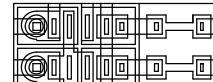
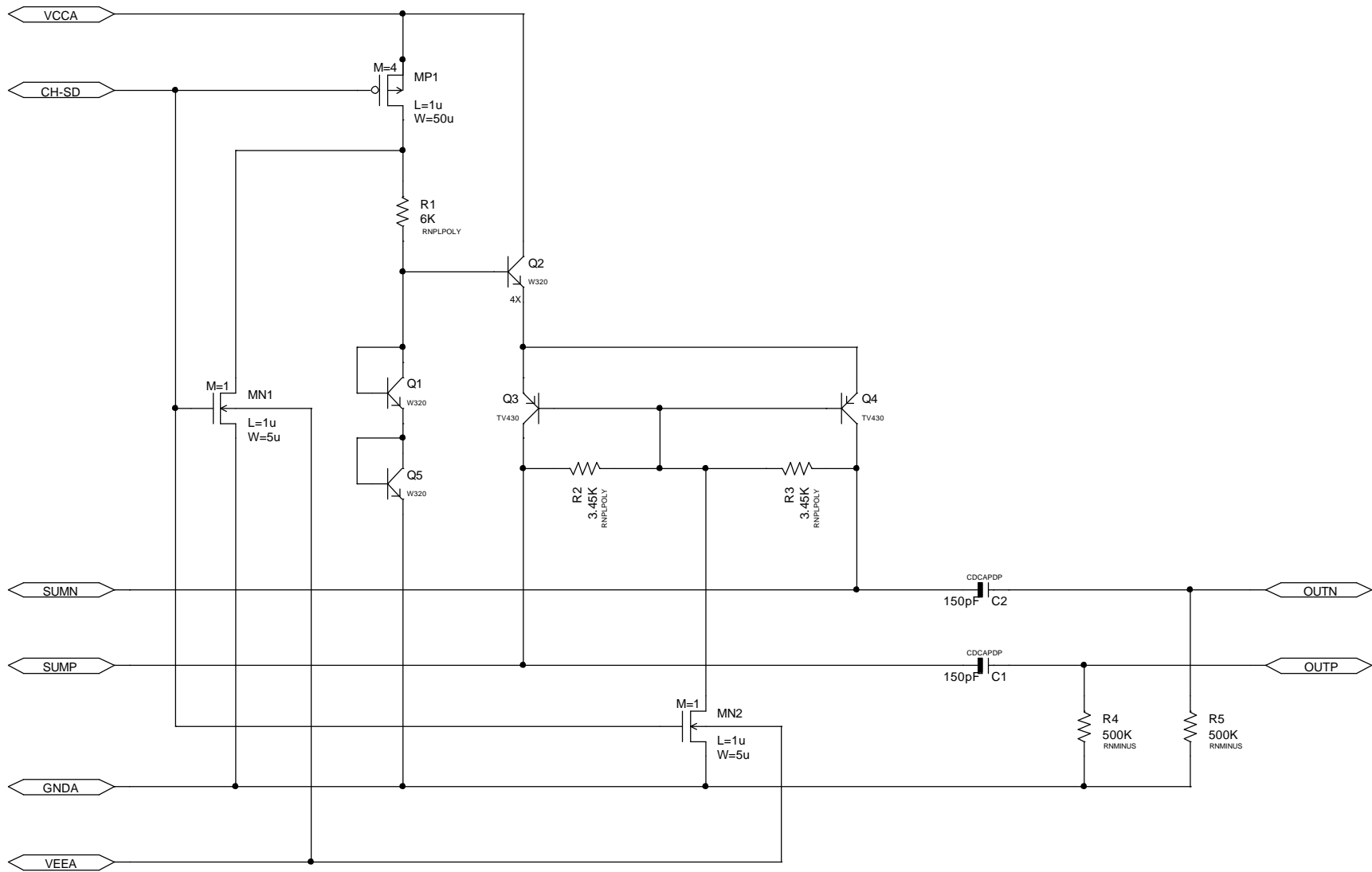
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Title: Frontend TVG (RevK: CHSELLOGIC Removed)		
Size B	FileName: ...FRONTEND-RevK.sch	REV K
July 5, 2002, 11:24 AM		Sheet 1 of 1



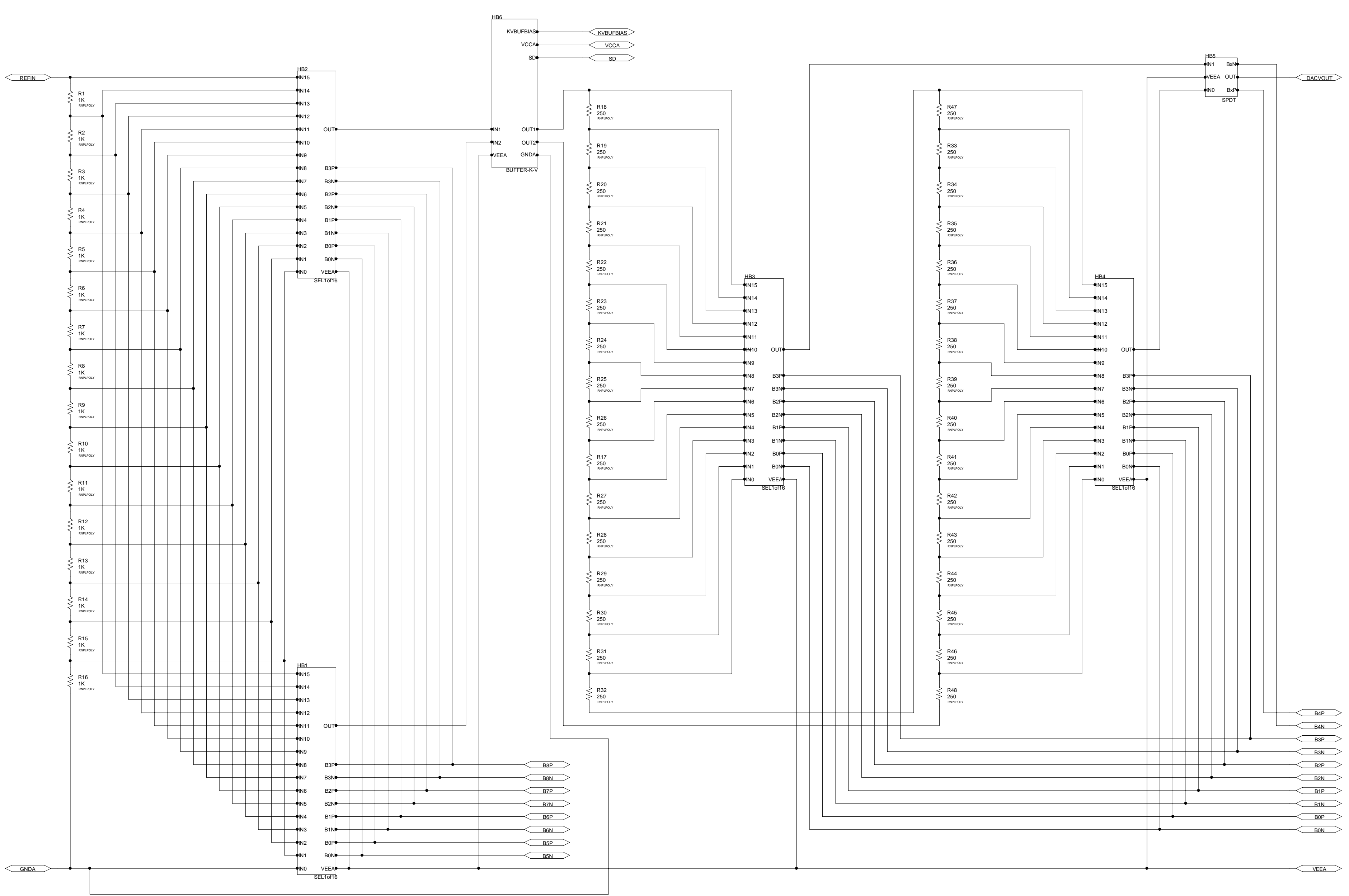
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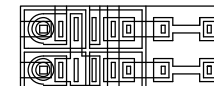
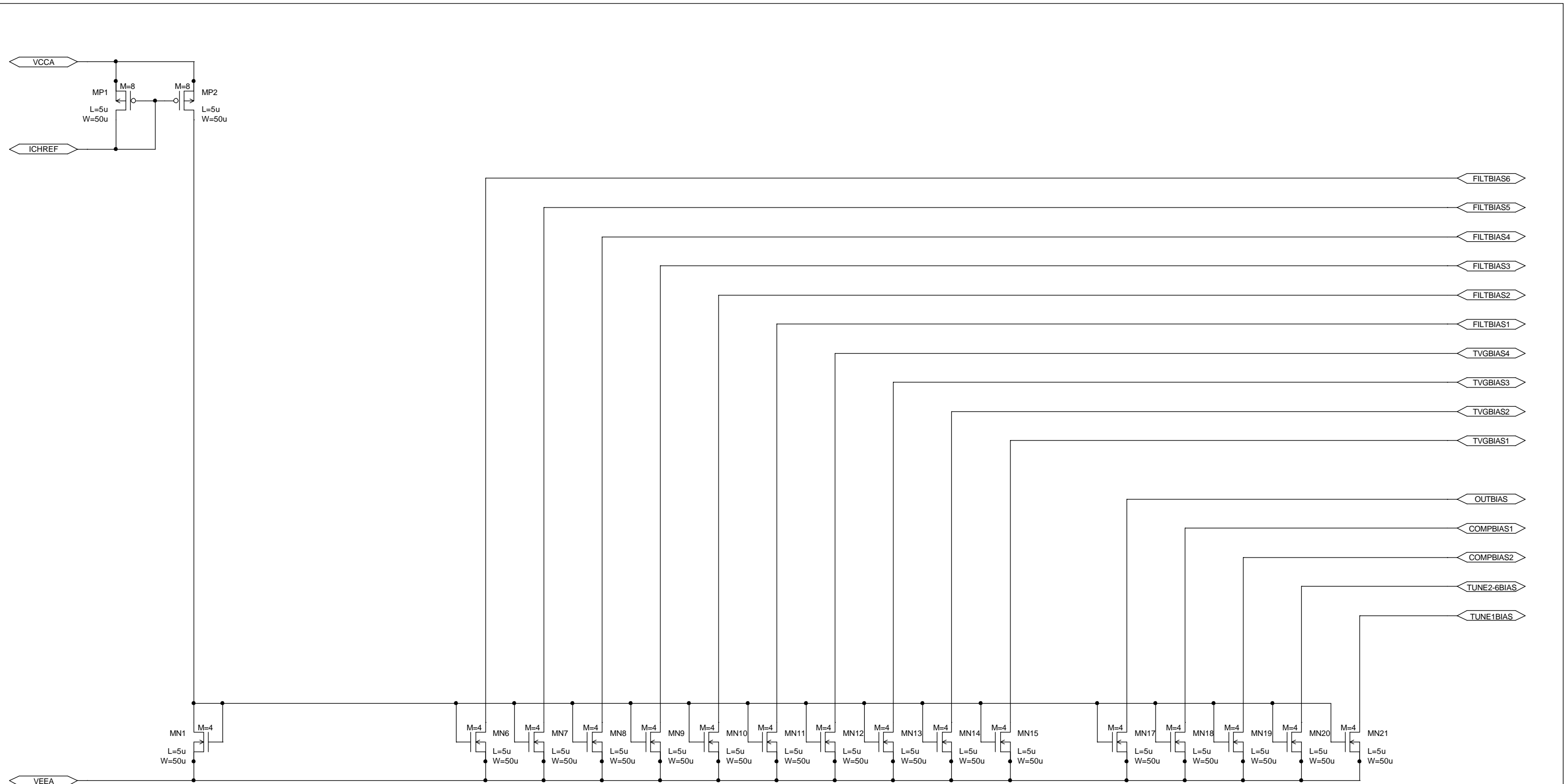
Title: Front Lump		
Size A	FileName: ...\FrontLump.sch	REV J
May 2, 2002, 9:55 AM		Sheet 1 of 1



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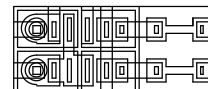
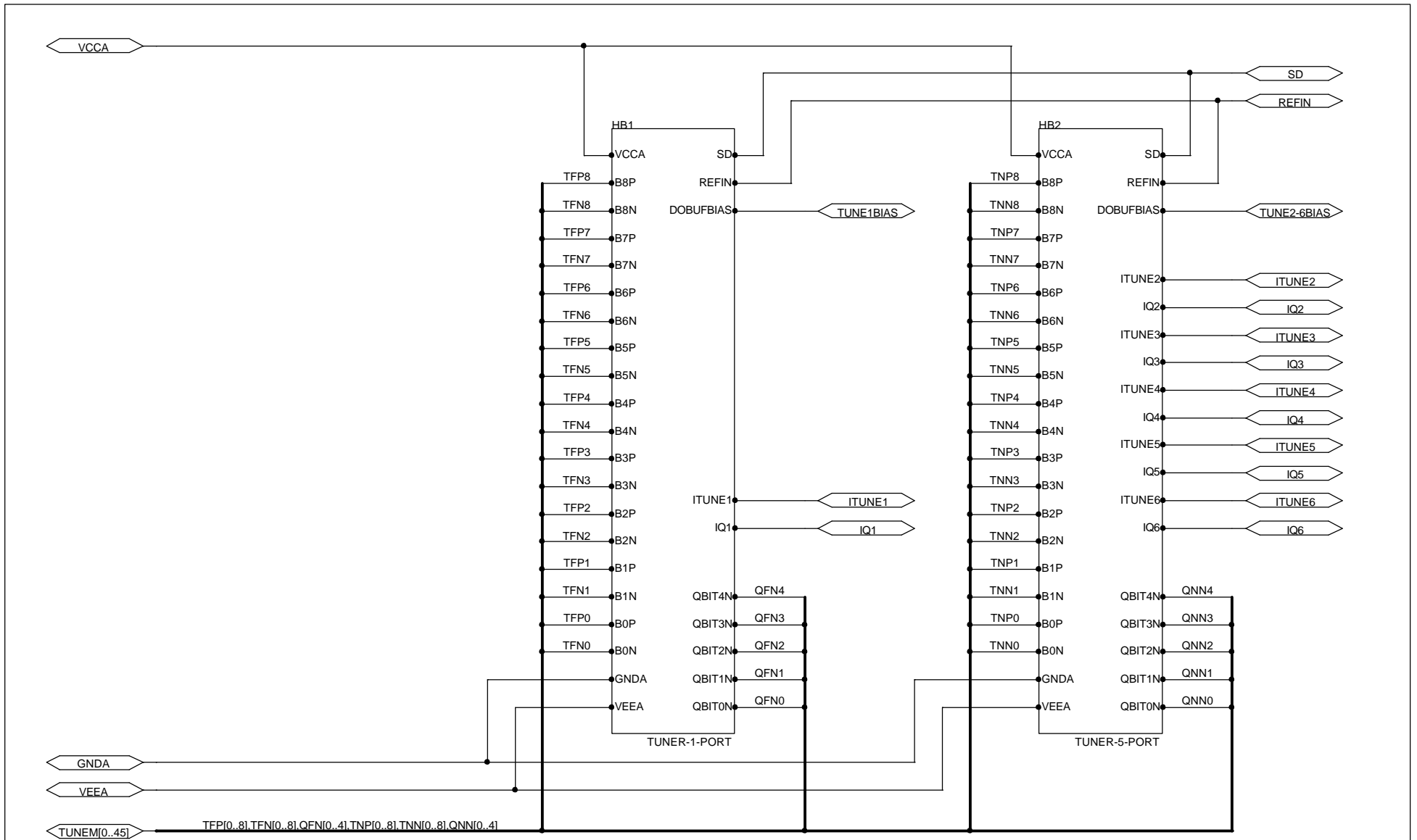
Title: Frontend Summation Module		
Size A	FileName: ...\FrontSum.sch	REV J
May 2, 2002, 9:55 AM		Sheet 1 of 1





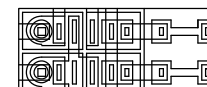
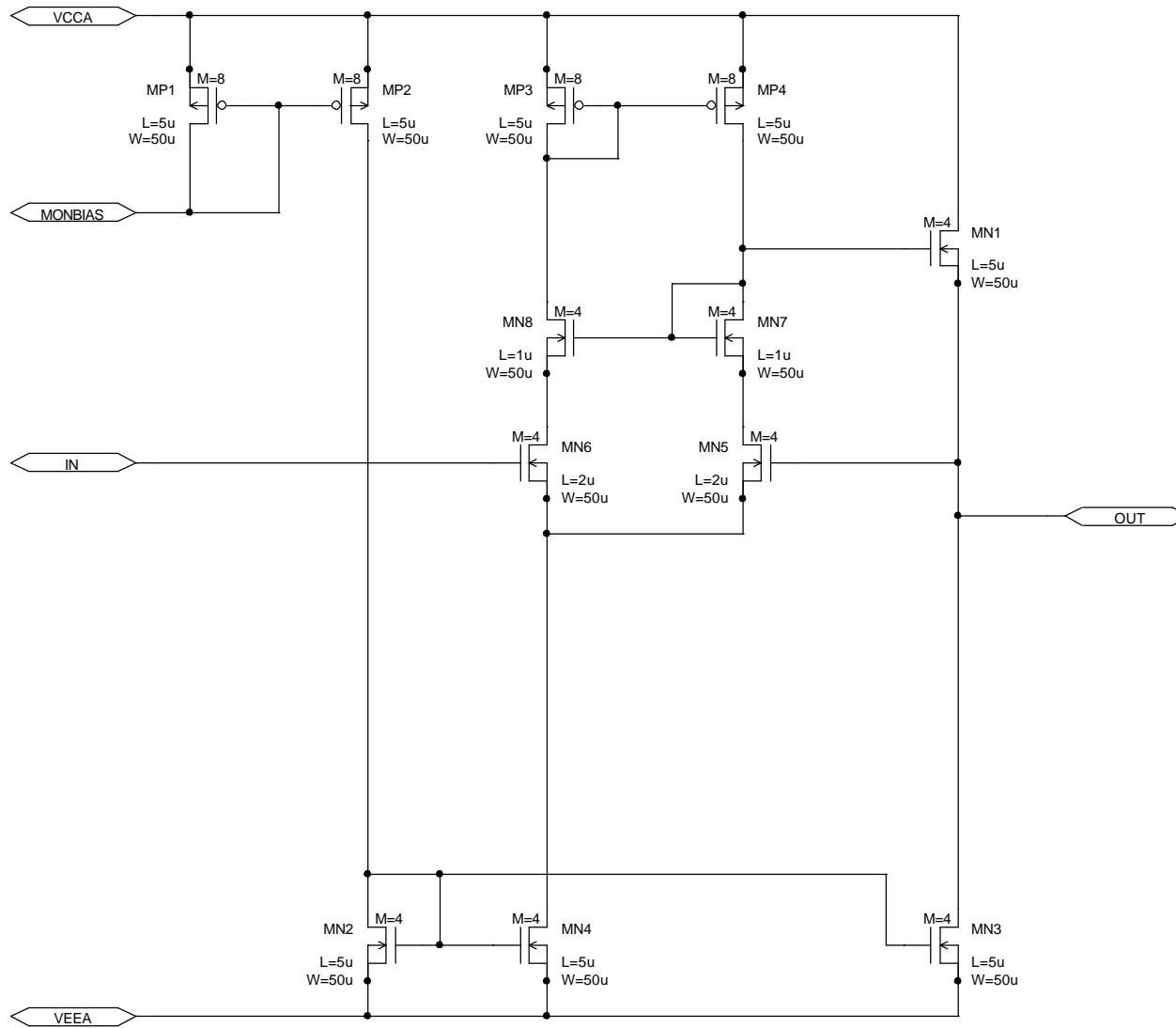
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Title: Channel Current Mirrors (Eliminate IF and Mixer Bias)		REV C
Size B	FileName: ...Local-Mirror-RevC.sch	
July 2, 2002, 3:31 PM		Sheet 1 of 1



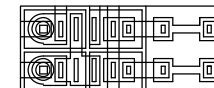
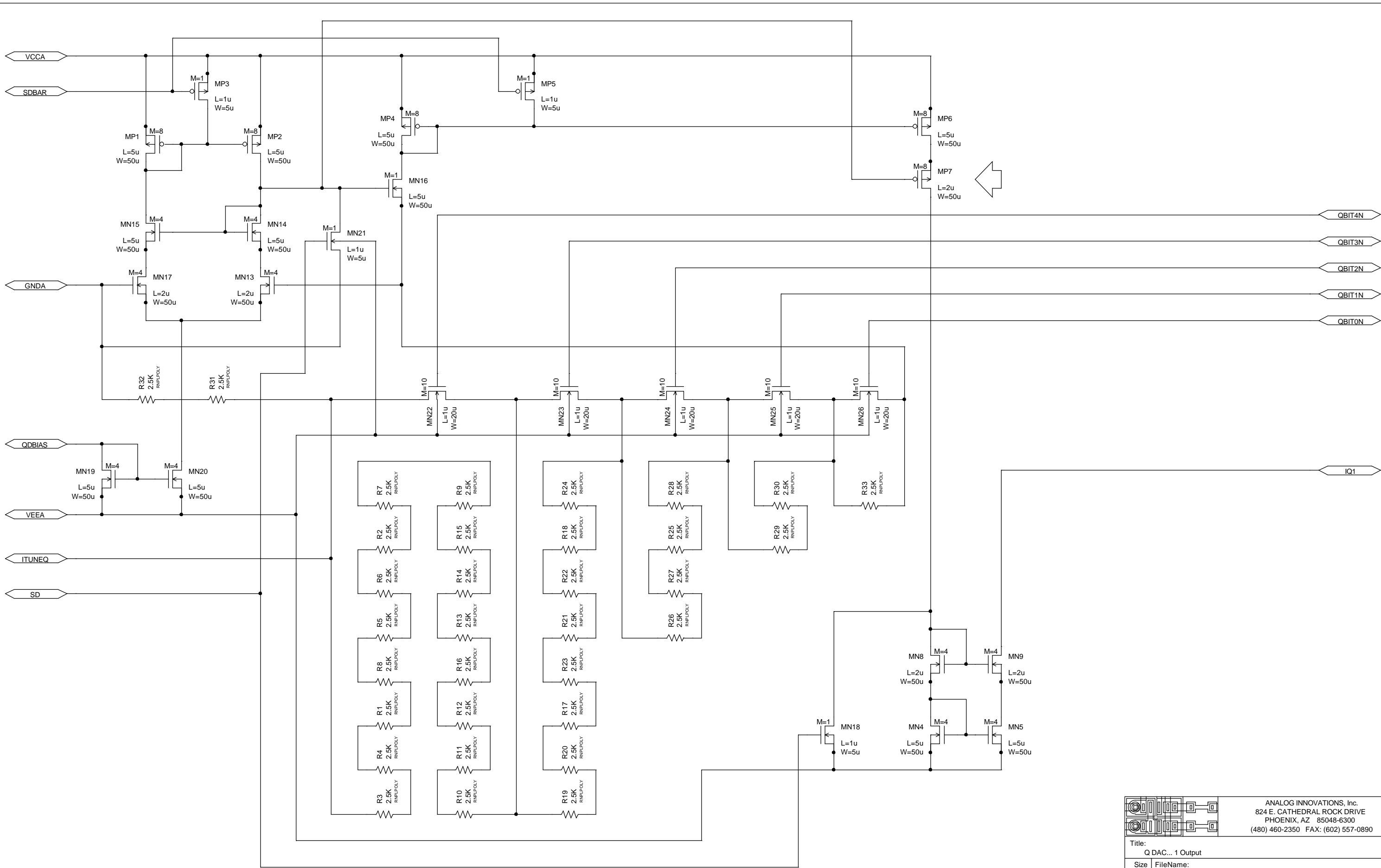
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Title: Main Tuner		
Size A	FileName: ...\MainTuner.sch	REV B
June 7, 2002, 2:46 PM		Sheet 1 of 1



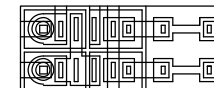
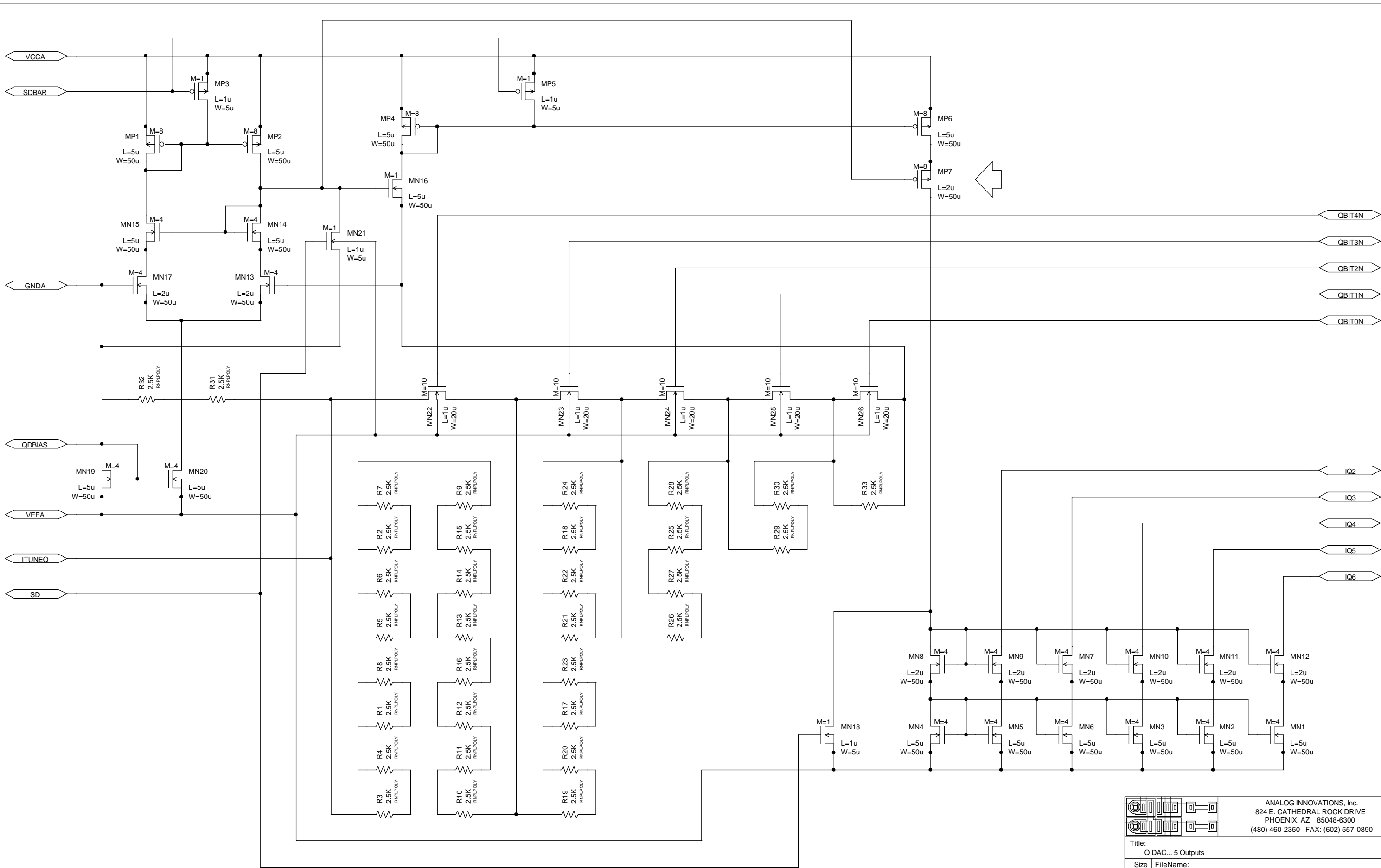
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Title: Monitor		
Size A	FileName: ...Monitor.sch	REV
November 8, 2001		Sheet 1 of 1



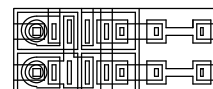
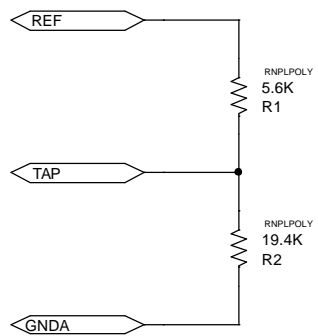
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Title: Q DAC... 1 Output		REV B
Size B	FileName: ...Q-DAC-1Port.sch	
June 2, 2002, 10:13 AM	Sheet 1 of 1	



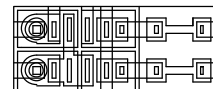
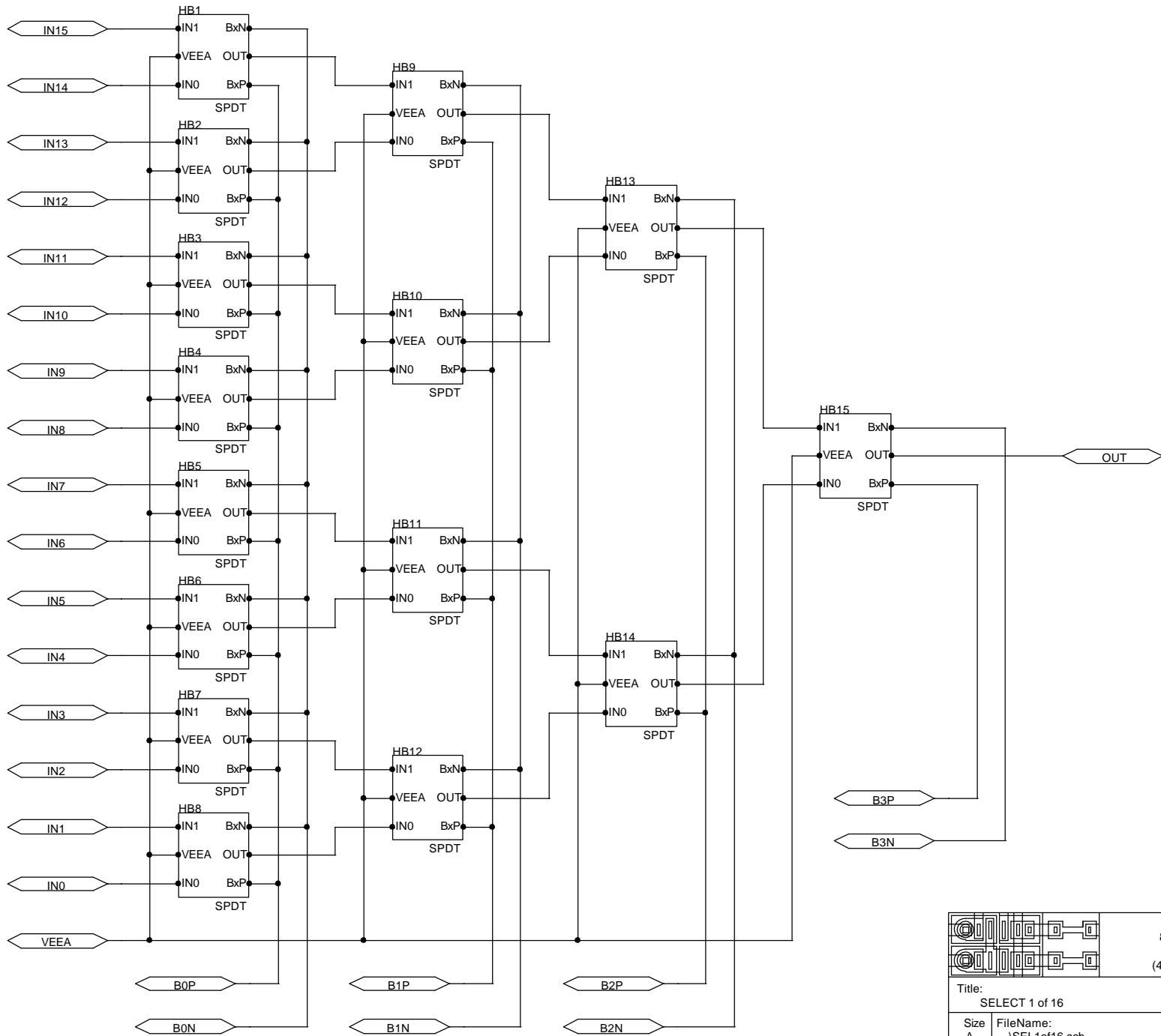
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Title: Q DAC... 5 Outputs		REV B
Size B	FileName: ...Q-DAC-5Port.sch	



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Title: Reference Divider for Gain Calibration		
Size A	FileName: ...\REFDIVIDER.sch	REV A
August 21, 2002, 4:23 PM		Sheet 1 of 1



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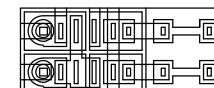
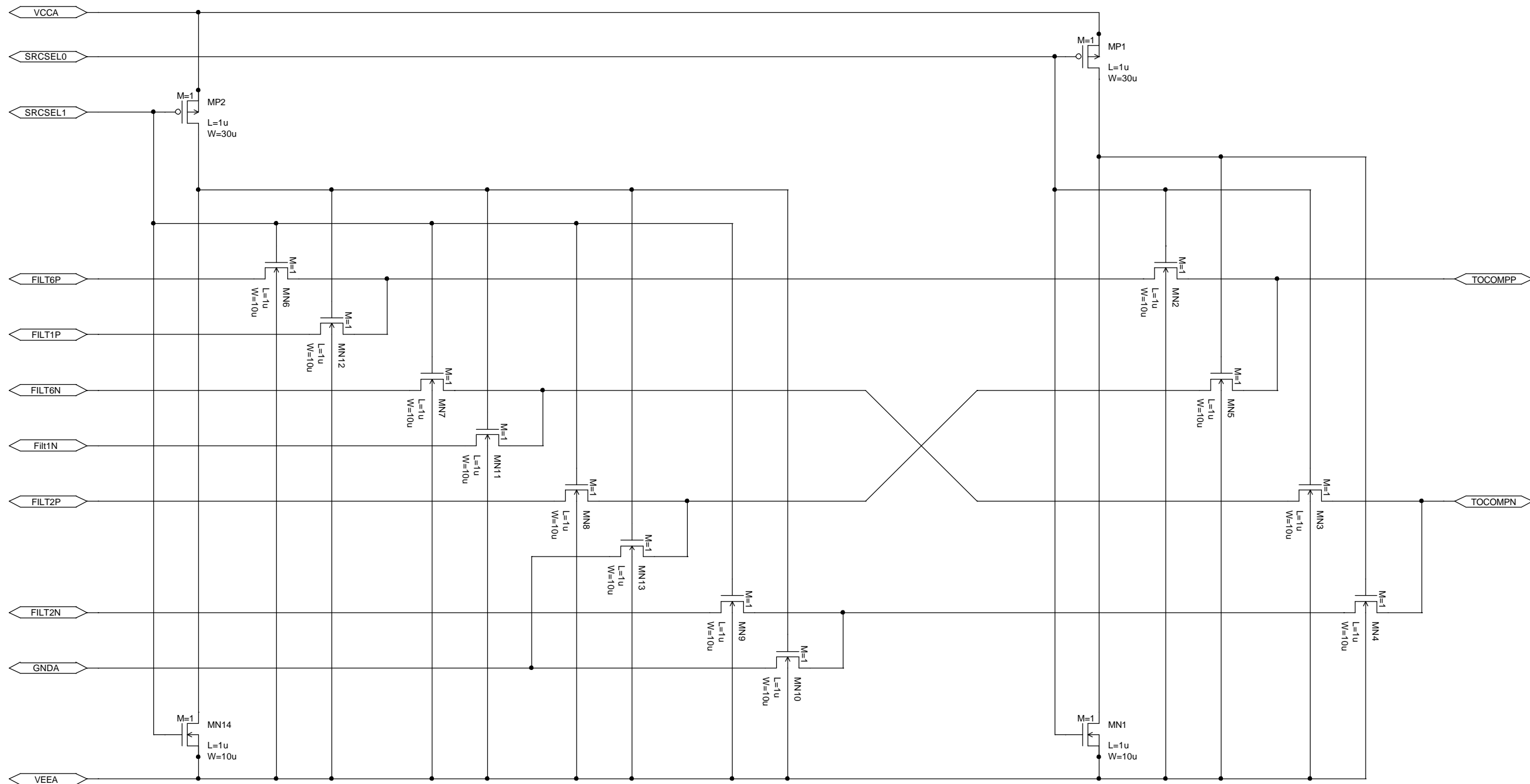
Title:
 SELECT 1 of 16

Size A
 FileName: ...SEL1of16.sch

REV
 A

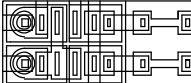
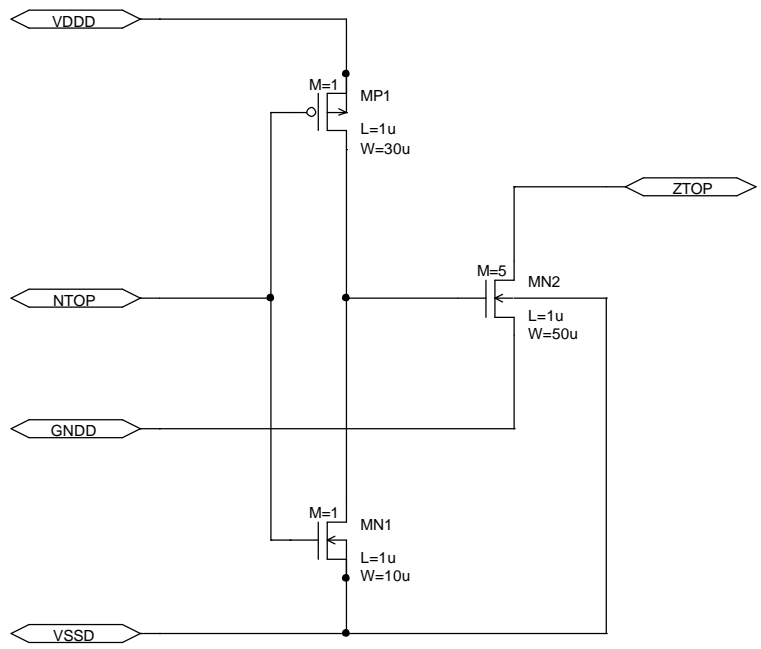
May 16, 2002, 8:22 AM

Sheet 1 of 1



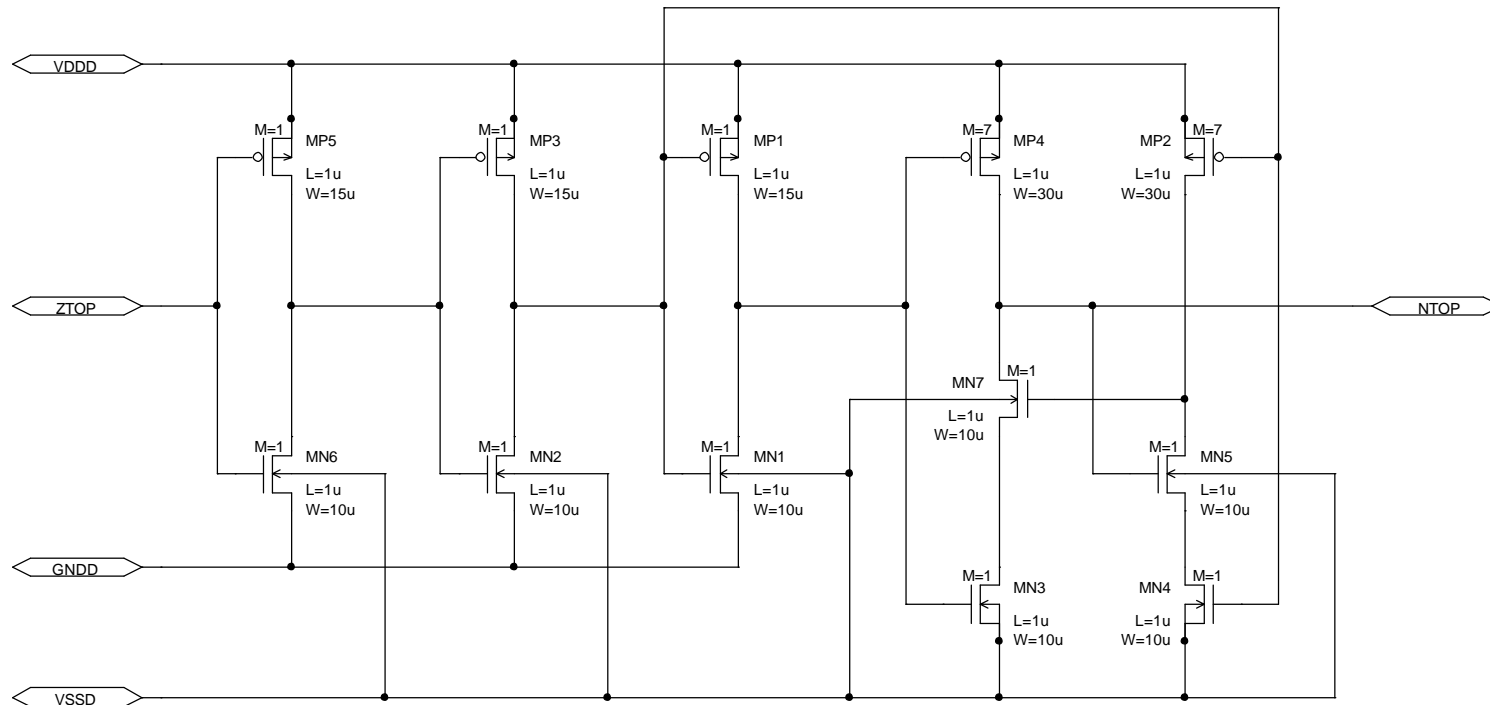
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Title: Calibration Source Selector		REV A
Size B	FileName: ...\SelCalSrc.sch	
July 4, 2002, 9:29 AM		Sheet 1 of 1



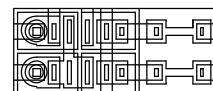
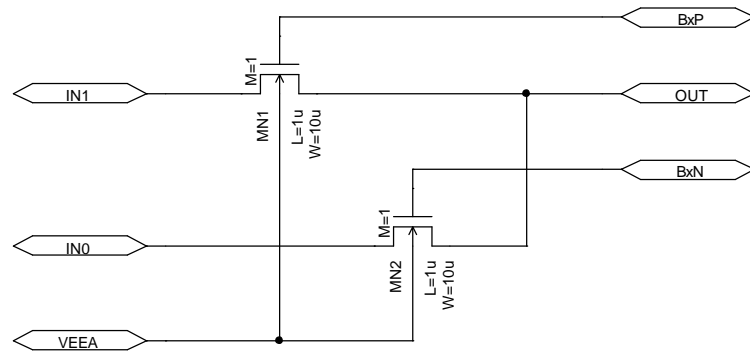
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Title: Level Shifter..FS to Open Drain		
Size A	FileName: ...SHIFT-NtoZ-OD.sch	REV A
April 16, 2002, 10:45 AM		Sheet 1 of 1



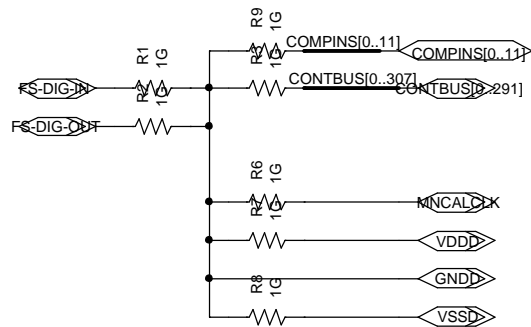
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Title: Level Shifter...0 <-> 3.3 to -2V <-> 3.3		
Size A	FileName: ...SHIFT-ZtoN.sch	REV A
November 30, 2001		Sheet 1 of 1

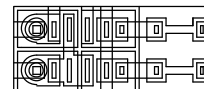


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Title: SPDT Switch		
Size A	FileName: ...\SPDT.sch	REV A
May 16, 2002, 9:28 AM		Sheet 1 of 1

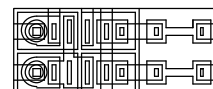
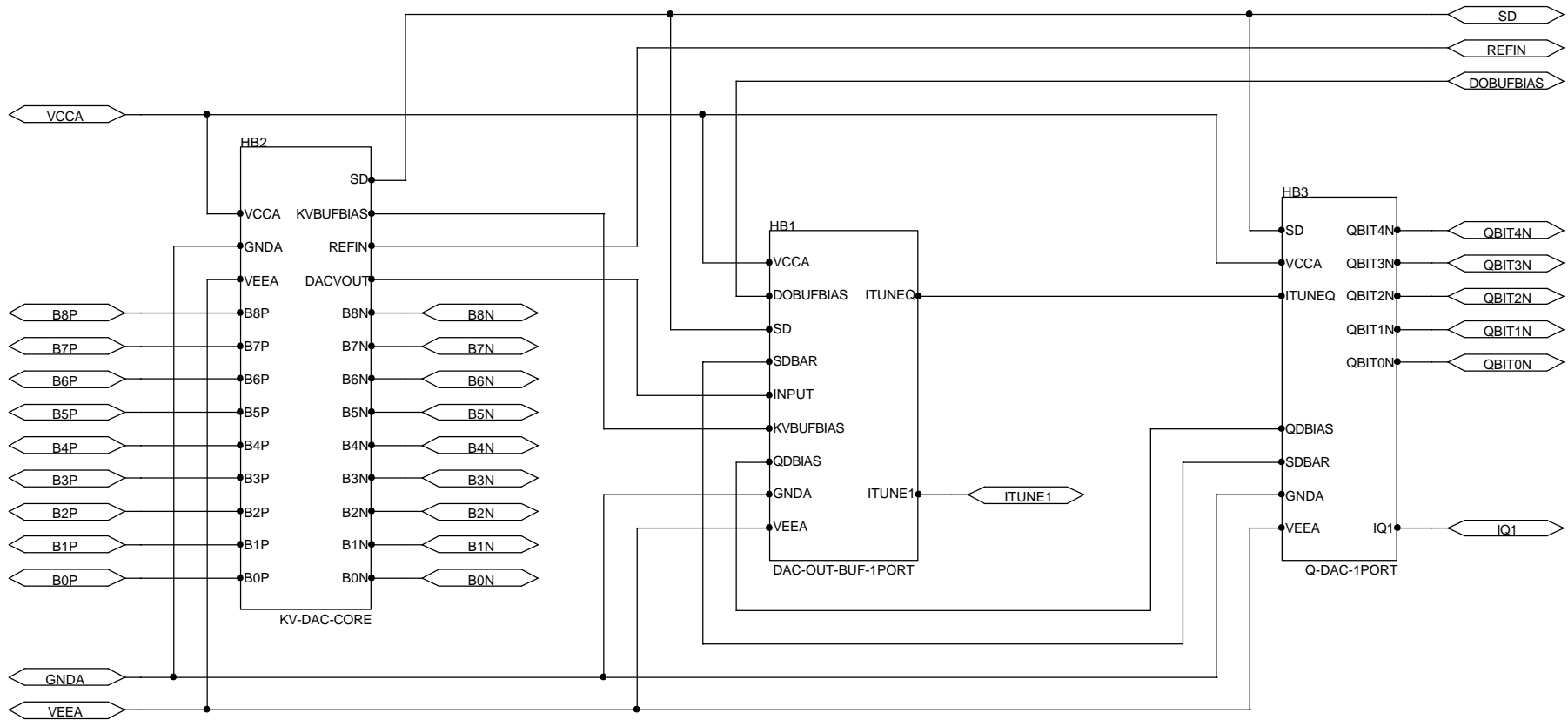


PLACEHOLDER



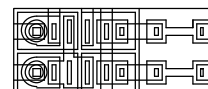
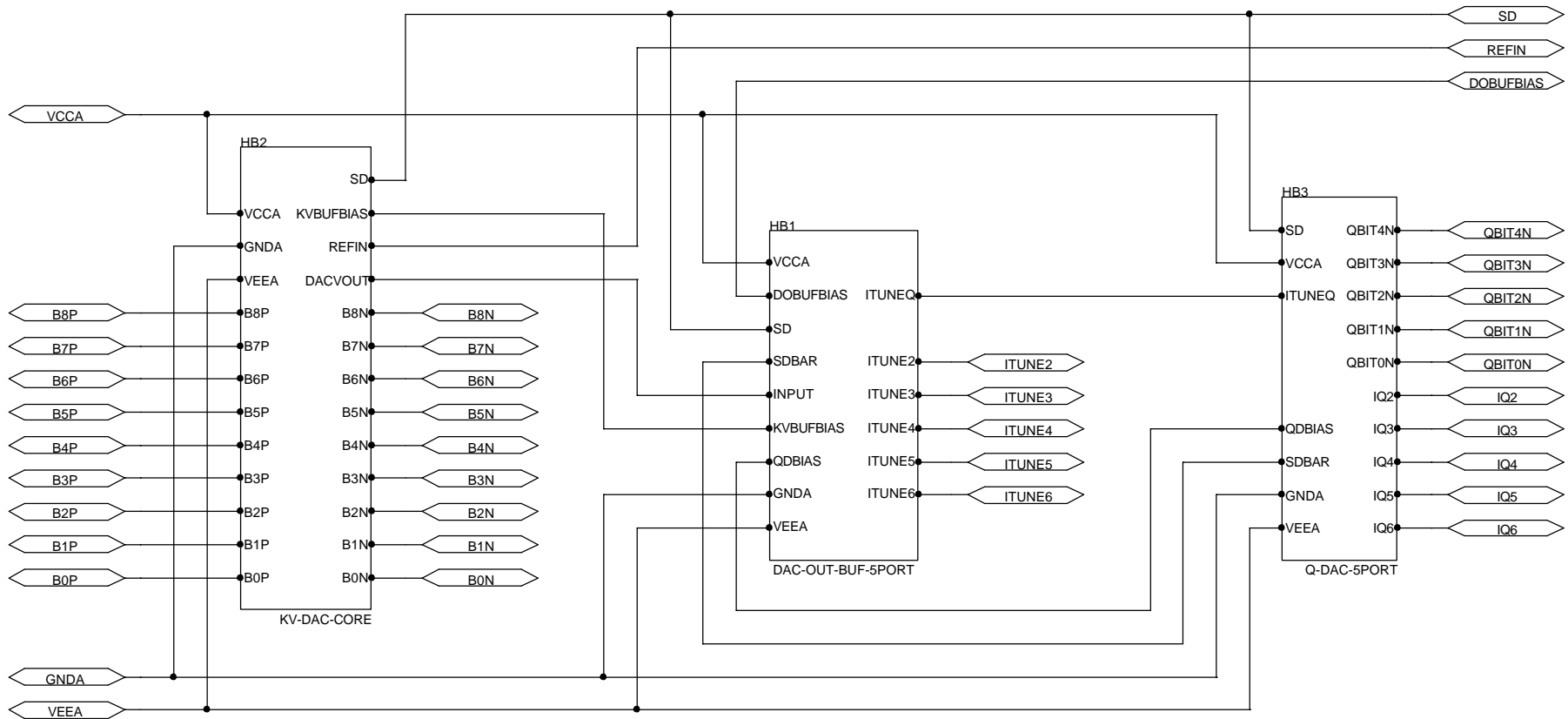
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Title: TITLE		
Size A	FileName: ...\ToddBlock.sch	REV A
April 16, 2002, 10:55 AM		Sheet 1 of 1



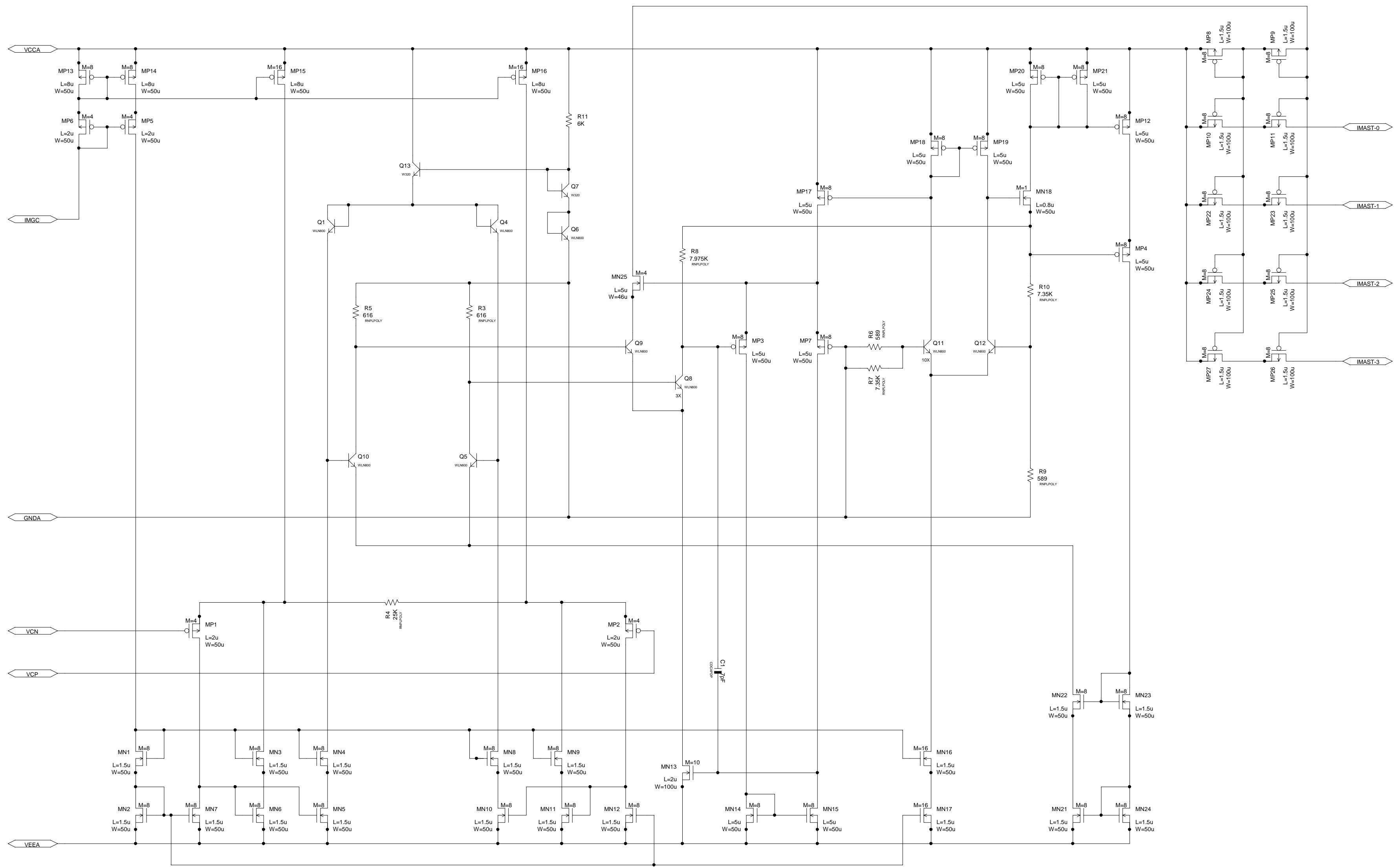
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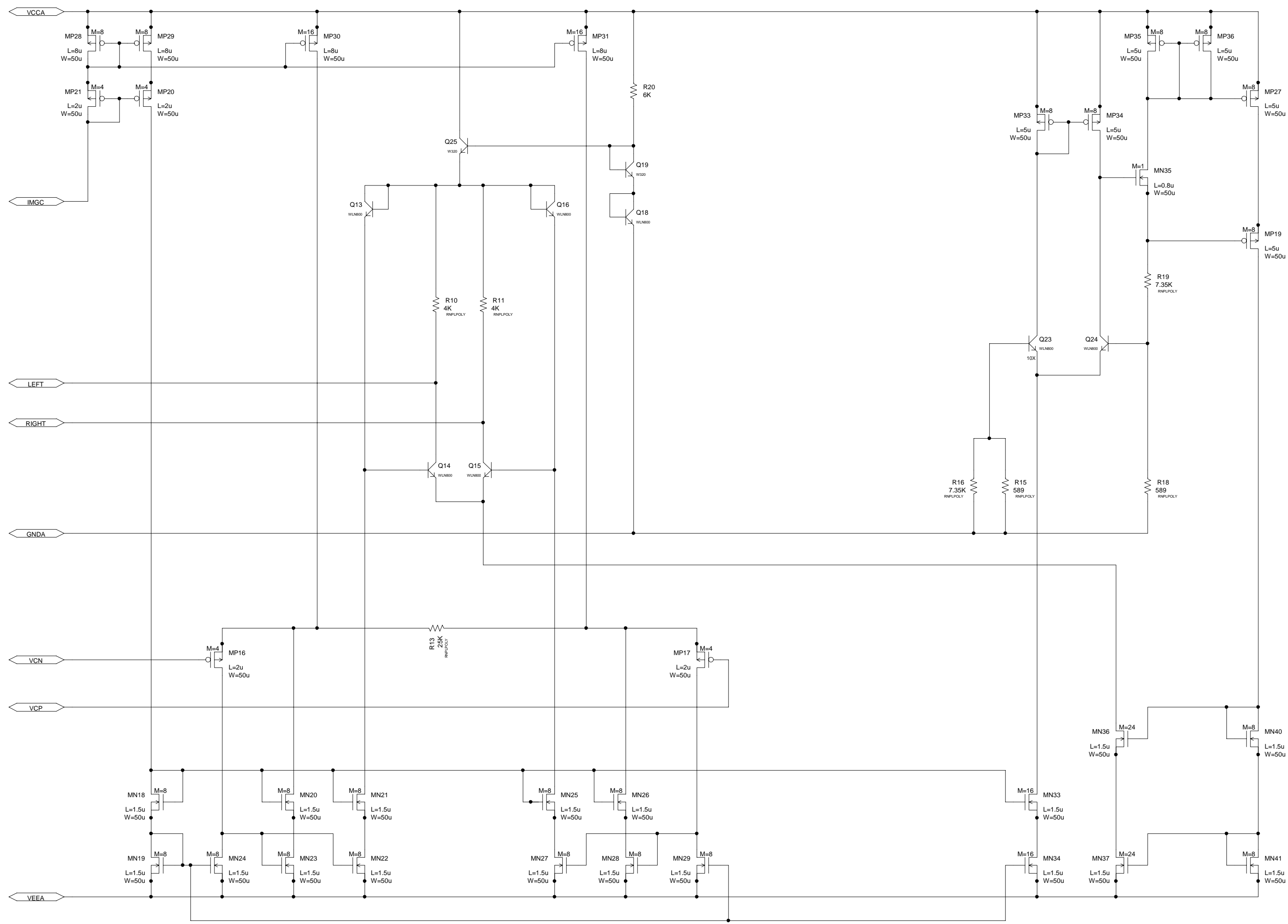
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Size A	FileName: ...\Tuner-1-Port.sch	REV A
June 1, 2002, 3:06 PM		Sheet 1 of 1

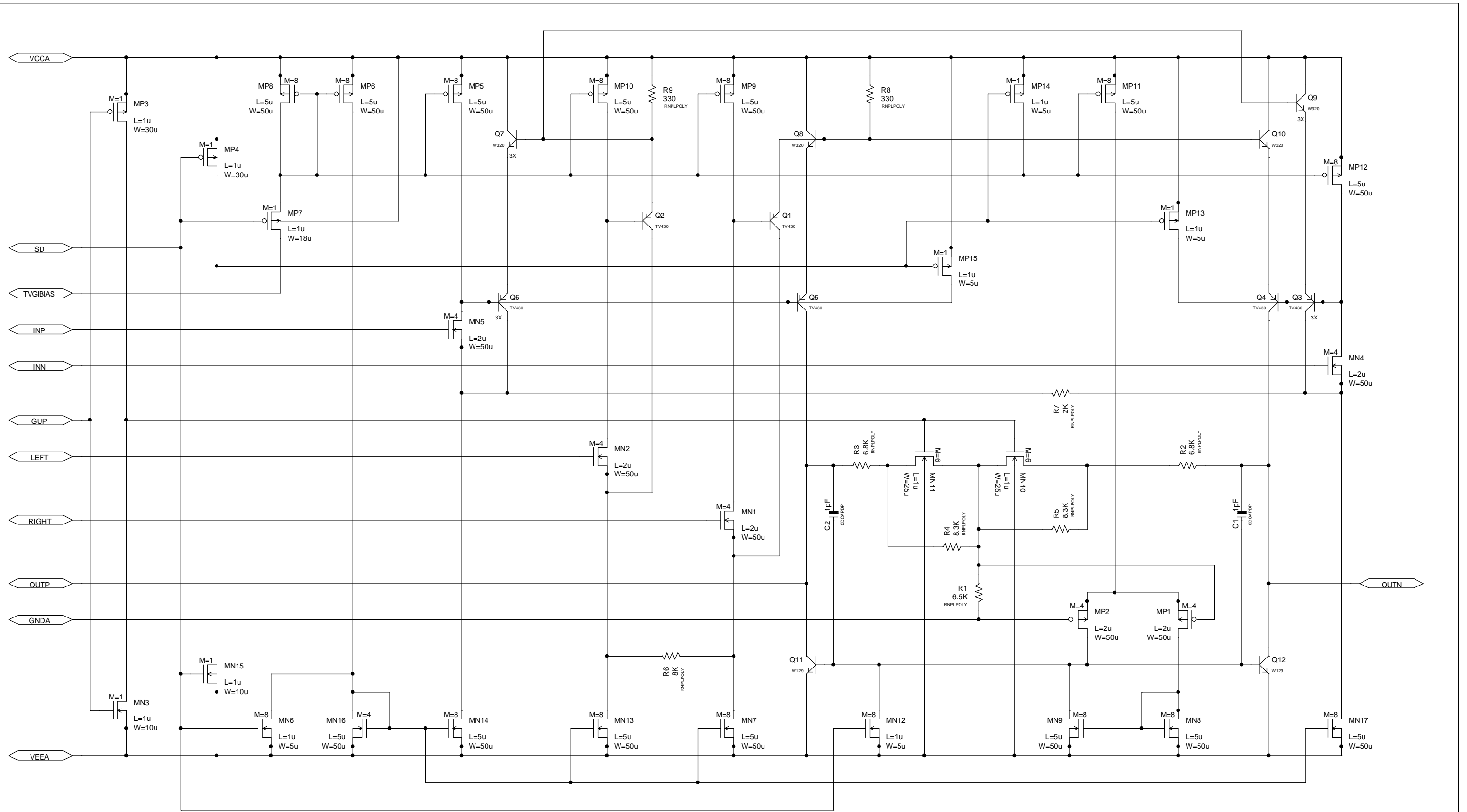


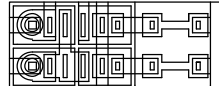
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Title: 5-Port Tuner		
Size A	FileName: ...\Tuner-5-Port.sch	REV A
June 1, 2002, 3:06 PM		Sheet 1 of 1







			ANALOG INNOVATIONS, Inc. 824 E. CATHEDRAL ROCK DRIVE PHOENIX, AZ 85048-6300 (480) 460-2350 FAX: (602) 557-0890
Title: TVG for Inside Application			
Size: B	FileName: ...TVG-Inner-CELL-RevJ.sch	REV: J	
May 2, 2002, 9:56 AM		Sheet 1 of 1	

DIGITAL CONTROLS, SPI BUS, etc, for this chip were created by an associate ...

Todd James
2713 Skelton Lane
Blacklick, OH 43004
(614)855-2741

Todd also did the chip layout.

I have been working with Todd for nearly 20 years. We first met when he was a grad student at Ohio State University, and he was working part-time for a company named Micrys.

Todd is expert in VHDL, Verilog and the use of Cadence layout and simulation tools.

Feel free to contact him directly for any of that sort of work.

His digital techniques will not be divulged here... so this page is only a place-holder ☺

Click the smiley to return to the originating page.