

Transistor sensor needs no compensation

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The thermometer circuit in Fig 1 uses an inexpensive transistor to accurately measure temperature without compensation or calibration. Almost all transistor sensors use the base-emitter diode's voltage-shift with temperature as their sensing mechanism. Unfortunately, the *absolute* diode voltage is unpredictable, necessitating circuit calibration each time you fit a new transistor sensor.

The circuit in Fig 1 overcomes this limitation. The circuit provides a 0-to-10V output corresponding to a 0-to-100°C input. Unadjusted error is $< \pm 1\%$.

The basis for the circuit is the predictable relationship between current and voltage in a transistor's V_{BE}

junction. At room temperature, the V_{BE} junction diode shifts 59.16 mV per decade of current. The temperature dependence of this constant is $0.33\%/^{\circ}\text{C}$, or $198 \mu\text{V}/^{\circ}\text{C}$. The ΔV_{BE} -vs-current relationship holds, regardless of the V_{BE} diode's *absolute* value.

An internal oscillator controls the state of the switches in IC₁, the LTC1043. The 0.01- μF capacitor at pin 16 sets the IC's oscillator frequency at about 500 Hz. Q₁ operates as a switched-value current source, alternating between about 10 and 100 μA as IC₁ commutates switch pins 12 and 14. The two currents' exact values are unimportant, so long as their *ratio* remains constant.

Because of this constant ratio, Q₁ requires no reference, although its emitter resistor's ratio must be precise. The alternating 10/100- μA stepped current drive

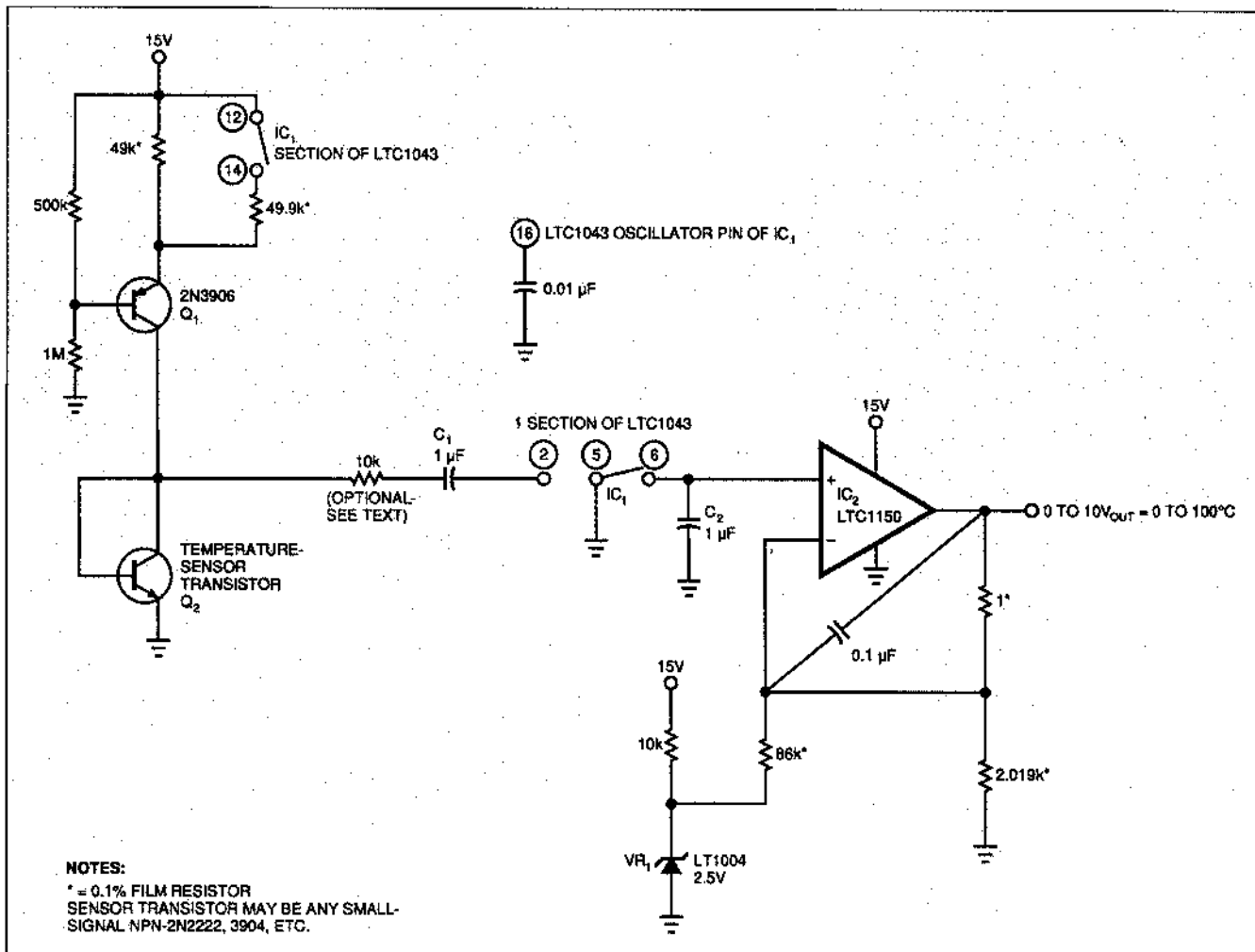


Fig 1—The transistor Q₂ senses temperature. This circuit requires no compensation, even if you change transistors.

DESIGN IDEAS

to the sensor transistor, Q_2 , causes the theoretical 59.16-mV excursion at 25°C to appear across the V_{BE} junction.

C_1 couples this signal to a switched demodulator that strips off Q_2 's dc bias. Thus IC_1 's pin 2 sees only the 59-mV waveform, which the demodulator action at pins 5 and 6 references to ground. Pin 5, connected to capacitor C_2 , sits at pin 2's peak dc value. IC_2 amplifies this dc signal, with VR_1 providing offset so that 0°C equals 0V output. The optional 10-k Ω resistor protects against ESD (electrostatic discharge) events, which may occur if Q_2 is at the end of a cable.

Using the components in Fig 1, the circuit achieves $\pm 1\%$ error over a sensed 0-to-100°C range. Substituting randomly selected 2N3904s and 2N2222s for Q_2

showed less than 0.4°C spread over 25 devices from various manufacturers. (EDN BBS /DL_SIG #945)

EDN

Reference(s)

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2. Type 7013 Plug-In Operating and Service Manual, Tektronix Inc, 1971.
3. Sheingold, D H, "Non-Linear Circuits Handbook," Chapter 3-1, *Basic Considerations*, pp 165-166, Analog Devices Inc, 1974.

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Feedback tames detector overshoot

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The peak detector in Fig 1 employs positive feedback, rather than using phase compensation or reducing the circuit's feedback factor (increasing gain), to control overshoot. A peak detector must control overshoot because uncontrolled overshoot leads to errors of 30% or more. Using positive feedback for control expands your choice of op amps beyond those that allow only external compensation.

Resistors R_1 and R_2 provide the necessary positive feedback. Op amp IC_1 buffers and charges the holding capacitor, C_H . Voltage follower IC_2 isolates the hold capacitor from the load. A feedback loop removes IC_2 's errors from the output.

Diode D_1 switches the feedback loop to control peak detecting. As long as the voltage on C_H is higher than the input, D_1 is reverse-biased, and the feedback loop is open. When the input rises above the voltage on C_H , IC_1 charges the holding capacitor to this new value and D_1 switches on the feedback loop, ensuring an accurate stored voltage on C_H .

Without overshoot, the circuit's error is just the input error of IC_1 ($\sim V_{OS} + V_{IN}/A$). But three factors make peak detectors prone to overshoot: normal op-amp overshoot, capacitive output loading, and having two amplifiers in a feedback loop.

Most op amps have 50 to 60° of phase margin. This

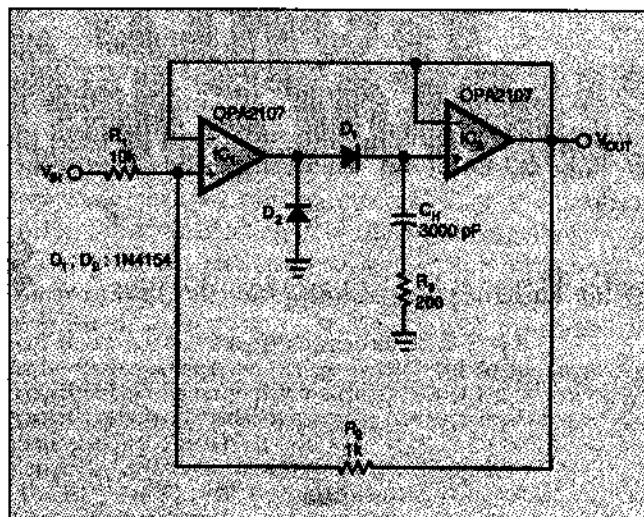


Fig 1—This peak detector's positive feedback reduces overshoot by reducing the circuit's feedback factor—without resorting to increased gain.

compensation offers the best settling time and best real-time accuracy for most applications. However, for peak detectors, this phase margin causes 10 to 15% overshoot. The inherent capacitive loading and the 2-op-amp design result in even greater overshoot.

The positive feedback via R_2 and R_1 has a positive feedback factor β equal to $R_1/(R_1 + R_2)$. This positive feedback combines with the unity negative feedback from the output of IC_2 to the negative input of IC_1 .

